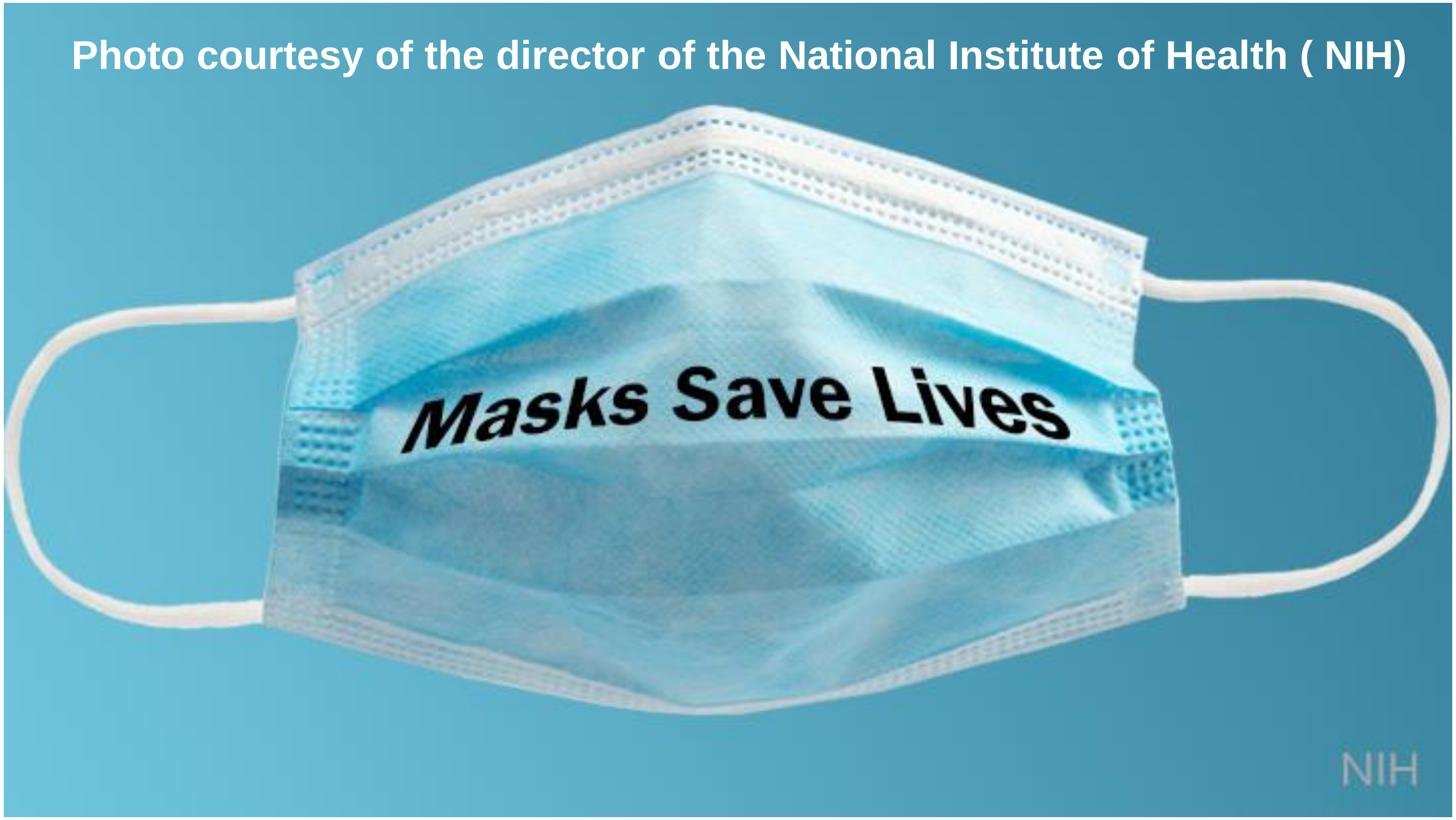
EE 330
Lecture 33

- High Gain Amplifiers
- Current Source Biasing
- Current Sources and Mirrors

Exam Schedule

Exam 1	Friday Sept 24
Exam 2	Friday Oct 22
Exam 3	Friday Nov 19
Final	Tues Dec 14 12:00 p.m.

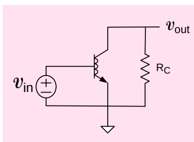
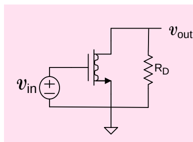
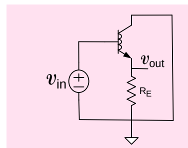
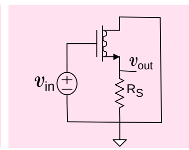
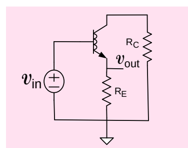
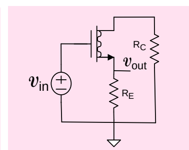
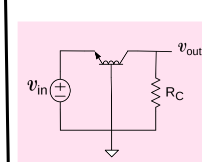
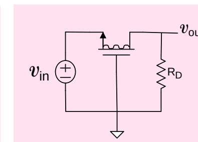
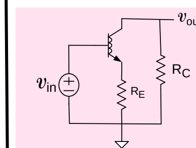
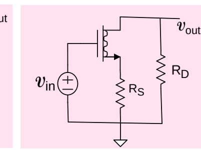


As a courtesy to fellow classmates, TAs, and the instructor

Wearing of masks during lectures and in the laboratories for this course would be appreciated irrespective of vaccination status

Review From Previous Lecture

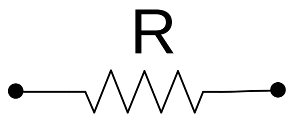
Basic Amplifier Application Gain Table

	CE/CS	CC/CD	CB/CG	CEwRE/CSwRS
	BJT  MOS 	BJT  MOS   	BJT  MOS 	BJT  MOS 
A_V	$-g_mR_C$ BJT: $-\frac{I_{CQ}R_C}{V_t}$ MOS: $-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{g_m}{g_m+g_E}$ BJT: $\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$ MOS: $\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	g_mR_C BJT: $\frac{I_{CQ}R_C}{V_t}$ MOS: $\frac{2I_{DQ}R_C}{V_{EB}}$	$-\frac{R_C}{R_E}$
R_{in}	r_π BJT: $\frac{\beta V_t}{I_{CQ}}$ MOS: ∞	$r_\pi+\beta R_E$ BJT: $\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$ MOS: ∞	g_m^{-1} BJT: $\frac{V_t}{I_{CQ}}$ MOS: $\frac{V_{EB}}{2I_{DQ}}$	$r_\pi+\beta R_E$ BJT: $\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$ MOS: ∞
R_{out}	R_C	g_m^{-1} BJT: $\frac{V_t}{I_{CQ}}$ MOS: $\frac{V_{EB}}{2I_{DQ}}$	R_C	R_C

(not two-port models for the four structures)

Can use these equations only when small signal circuit is EXACTLY like that shown !!

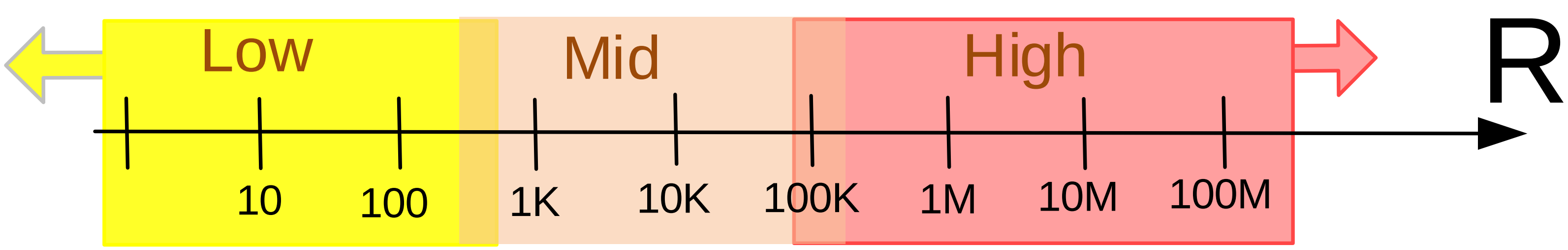
Impedance Range and Classification



The terms “High Impedance” and “ Low Impedance” are often used

Whether an impedance is considered high or low or mid-range is a relative assessment

When building MOS or BJT amplifiers, the following relative notation of impedance levels is often useful (though there may be some extreme applications where even this notation is not standard)



Impedance Range and Classification

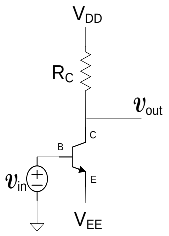
Ideal Port Impedance of the four basic amplifiers

Amplifier Type	R_{IN}	R_{OUT}
Voltage	∞	0
Current	0	∞
Transconductance	∞	∞
Transresistance	0	0

Review From Previous Lecture

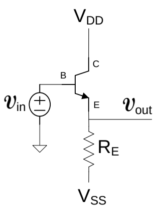
Basic Amplifier Characteristics Summary

CE/CS



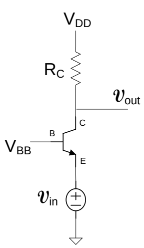
- **Large inverting gain**
- **Moderate input impedance**
- **Moderate (or high) output impedance**
- **Widely used as the basic high gain inverting amplifier**

CC/CD



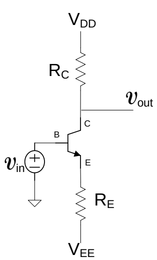
- **Gain very close to +1 (little less)**
- **High input impedance for BJT (high for MOS)**
- **Low output impedance**
- **Widely used as a buffer**

CB/CG



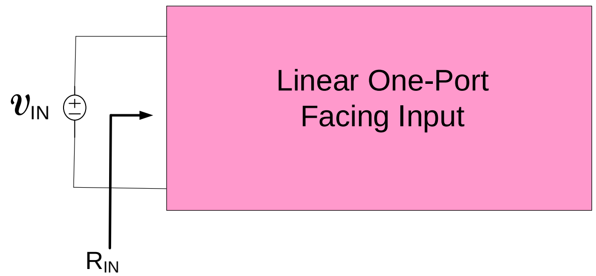
- **Large noninverting gain**
- **Low input impedance**
- **Moderate (or high) output impedance**
- **Used more as current amplifier or, in conjunction with CD/CS to form two-stage cascode**

CEwRE/
CSwRS

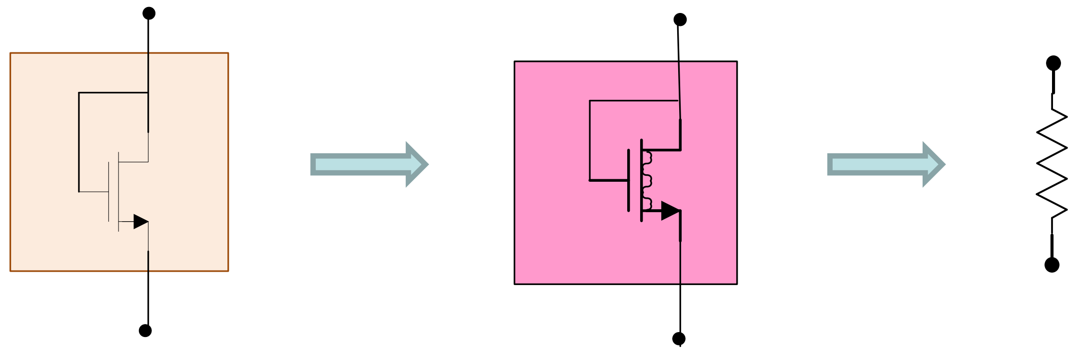


- **Reasonably accurate but somewhat small gain (resistor ratio)**
- **High input impedance**
- **Moderate output impedance**
- **Used when more accurate gain is required**

Review: Small-signal equivalent of a one-port

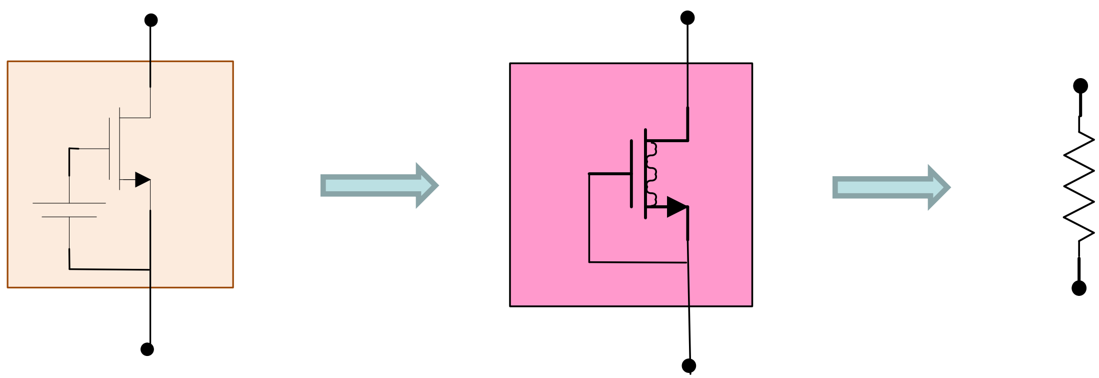


"Diode-connected transistor"



$$g = g_m + g_0 \approx g_m$$

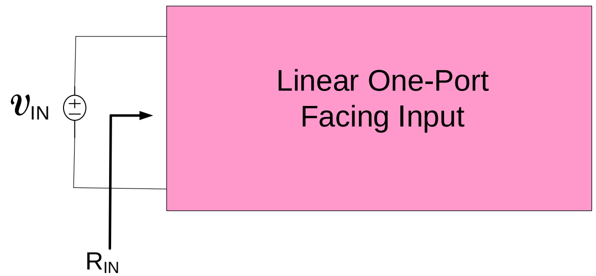
$$R = \frac{1}{g_m + g_0} \approx \frac{1}{g_m}$$



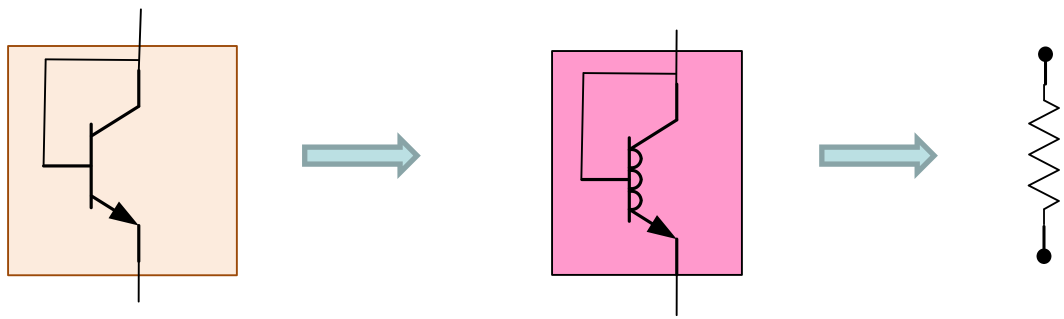
$$g = g_0$$

$$R = \frac{1}{g_0}$$

Review: Small-signal equivalent of a one-port

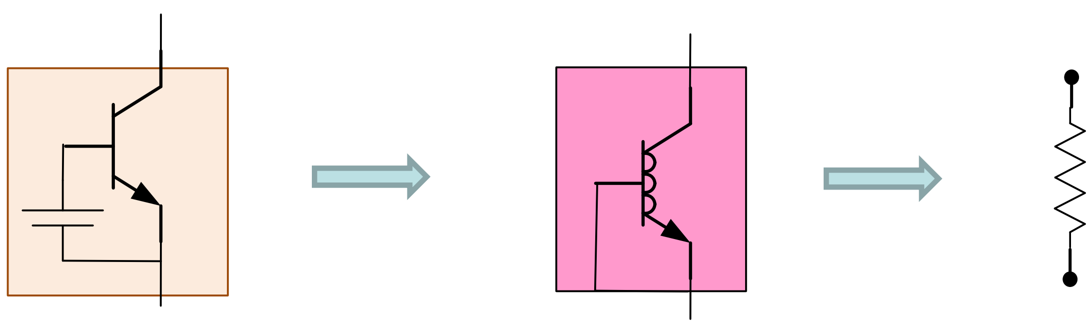


"Diode-connected transistor"



$$g = g_m + g_\pi + g_0 \approx g_m$$

$$R = \frac{1}{g_m + g_\pi + g_0} \approx \frac{1}{g_m}$$



$$g = g_0$$

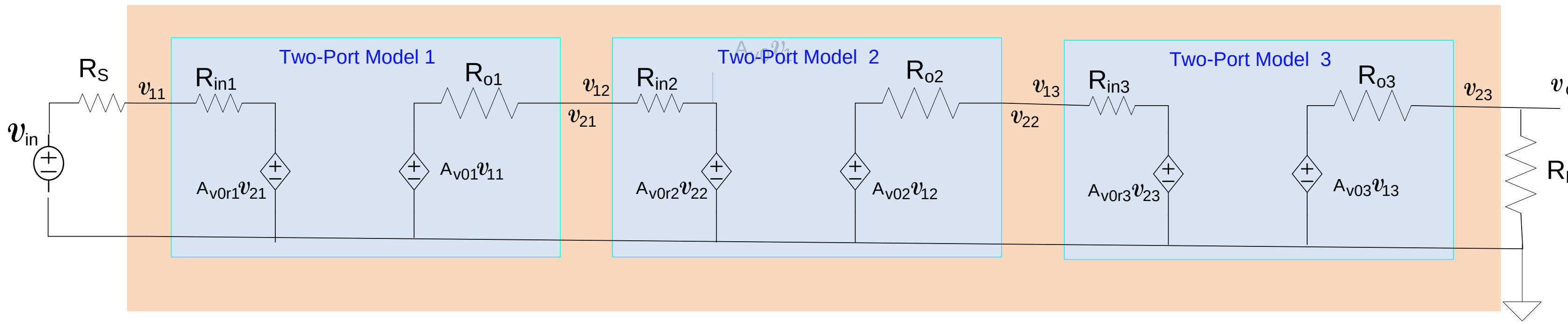
$$R = \frac{1}{g_0}$$

Review from Last Lecture

Cascaded Amplifier Analysis and Operation

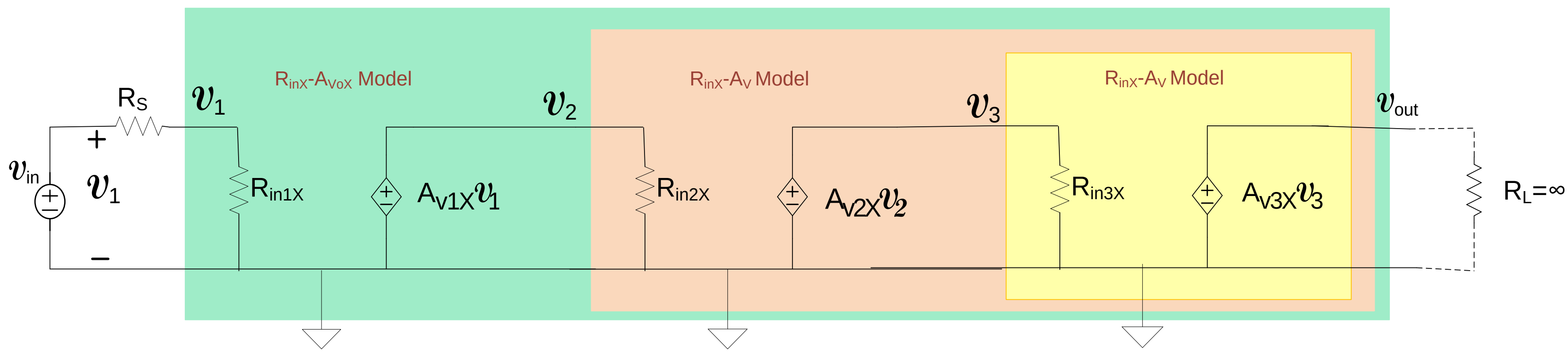
Case 2: One or more stages are not unilateral

- Standard two-port cascade



Analysis by creating new two-port of entire amplifier quite tedious because of the reverse-gain elements

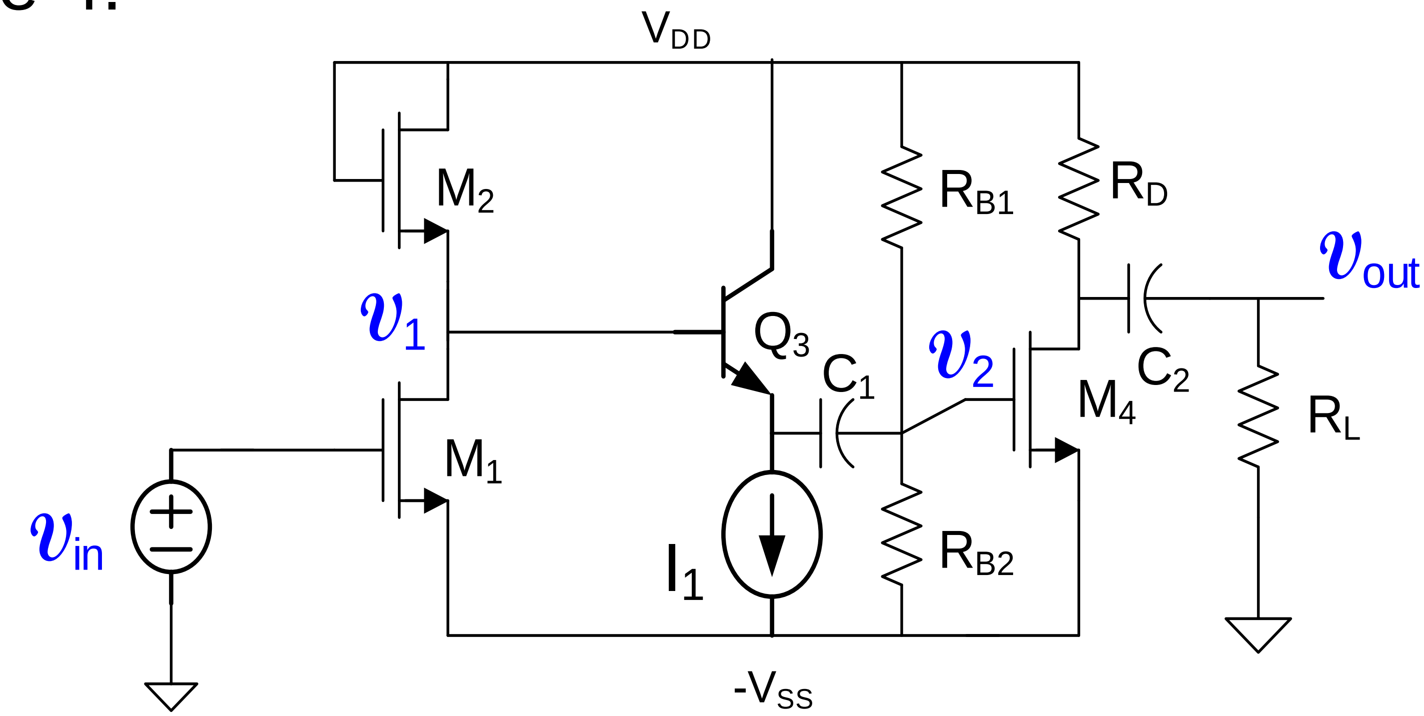
- Right-to-left nested R_{inx},A_{vX} approach



- R_{inx} includes effects of all loading
- AV_X is the voltage ratio from input to output of a stage
- AV_X's include all loading
- <u>Can not change any loading without recalculating everthing!</u>

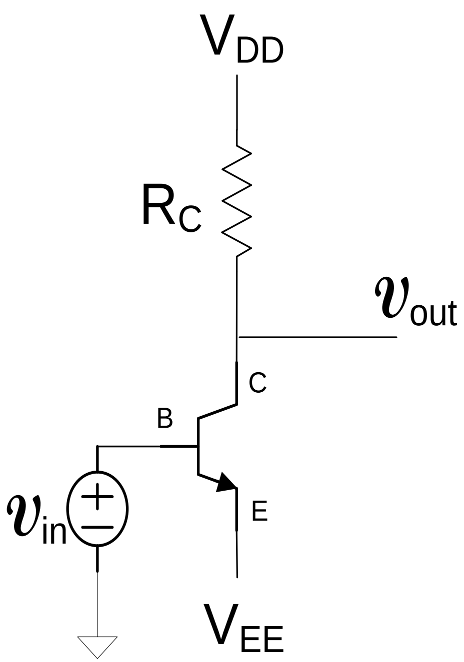
Review from Last Lecture

Example 4:



$$A_V = \frac{v_{out}}{v_2}\frac{v_2}{v_1}\frac{v_1}{v_{in}} \cong \left[-g_{m4}\left(R_D//R_L\right)\right]\left[1\right]\left[\frac{-g_{m1}}{g_{m2}+\left(\beta_3\left(R_{B1}//R_{B2}\right)\right)^{-1}}\right]$$

High-gain BJT amplifier



$$A_V = \frac{-g_m}{g_0 + G_C} \cong -g_m R_C$$

To make the gain large, it appears that all one needs to do is make R_C large !

$$A_V \cong -g_m R_C = \frac{-I_{CQ} R_C}{V_t}$$

But V_t is fixed at approx 25mV and for good signal swing, $I_{CQ}R_C<(V_{DD} - V_{EE})/2$

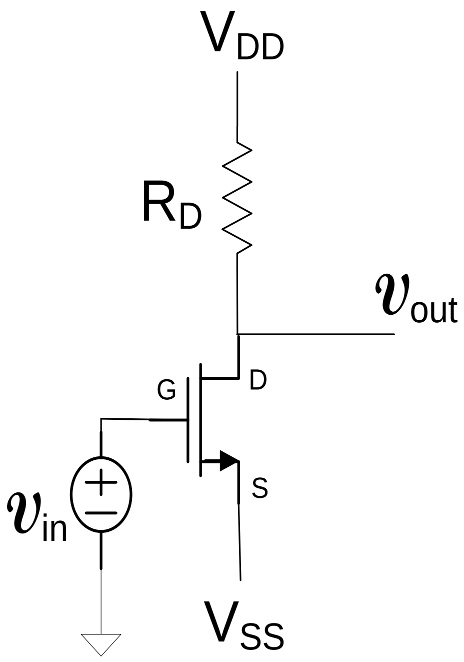
$$|A_V| < \frac{V_{DD} - V_{EE}}{2V_t}$$

If V_{DD}-V_{EE}=5V,

$$|A_V| < \frac{5V}{2 \bullet 25mV} = 100$$

- **Gain is practically limited with this supply voltage to around 100**
- **And in extreme case, limited to 200 with this supply voltage with very small signal swing**

High-gain MOS amplifier



$$A_V = \frac{-g_m}{g_0 + G_D} \cong -g_m R_D$$

To make the gain large, it appears that all one needs to do is make R_D large !

$$A_V \cong -g_m R_D = \frac{-2 I_{DQ} R_D}{V_{EB}}$$

But V_{EB} is practically limited to around 100mV and for good signal swing, $I_{DQ}R_D<(V_{DD}-V_{SS})/2$

$$|A_V| < \frac{V_{DD} - V_{SS}}{V_{EB}}$$

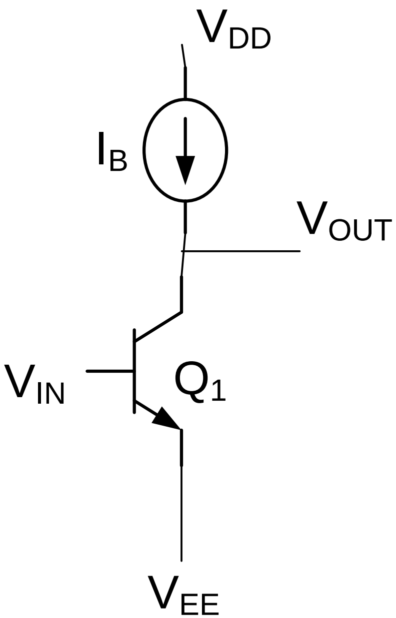
If V_{DD} -V_{SS}=5V and V_{EB}=100mV,

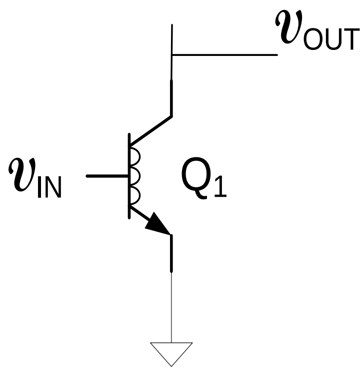
$$|A_V| < \frac{5V}{100mV} = 50$$

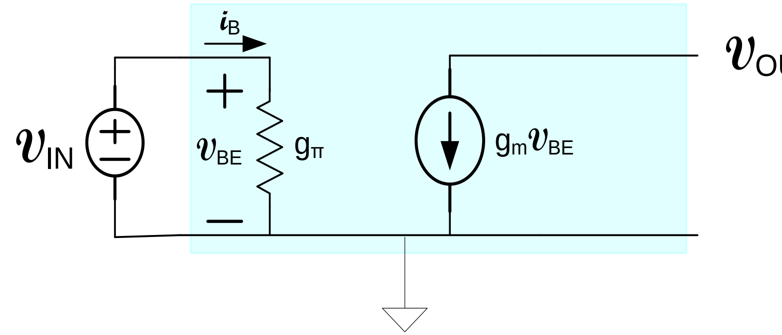
Gain is practically limited with this supply voltage to around 50

Are these fundamental limits on the gain of the BJT and MOS Amplifiers?

High-gain amplifier







$$A_V = \frac{-g_m}{0} = -\infty$$

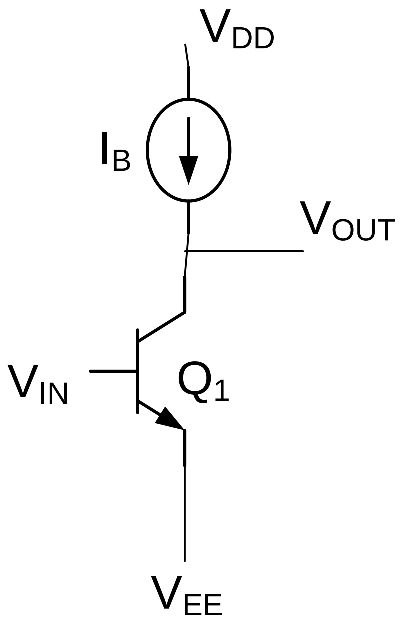
Fundamentally a different circuit

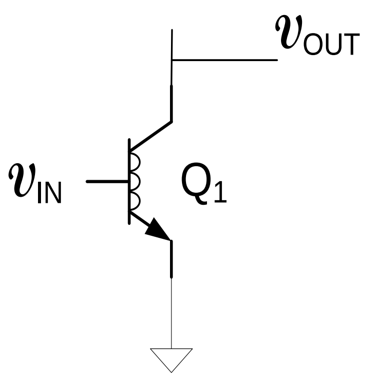
This gain is very large !

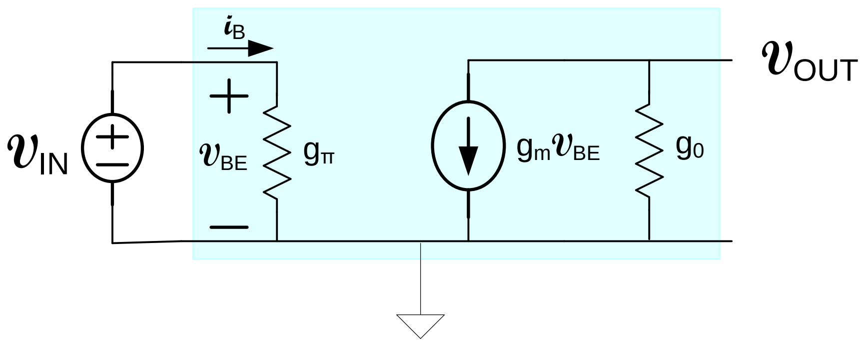
Too good to be true !

Need better model of BJT and MOS device (but we already have it) !

High-gain amplifier







$$A_V = \frac{-g_m}{g_0}$$

$$A_V = \frac{-I_{CQ}}{V_t I_{CQ}/V_{AF}} = -\frac{V_{AF}}{V_t}$$

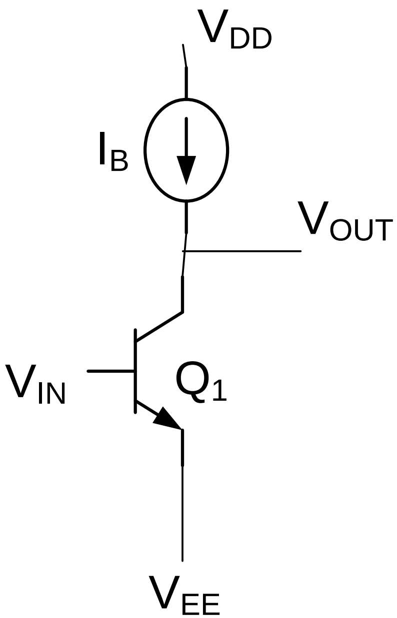
$$A_V = -\frac{V_{AF}}{V_t} \cong \frac{200V}{25mV} = -8000$$

This gain is very large (but realistic) !

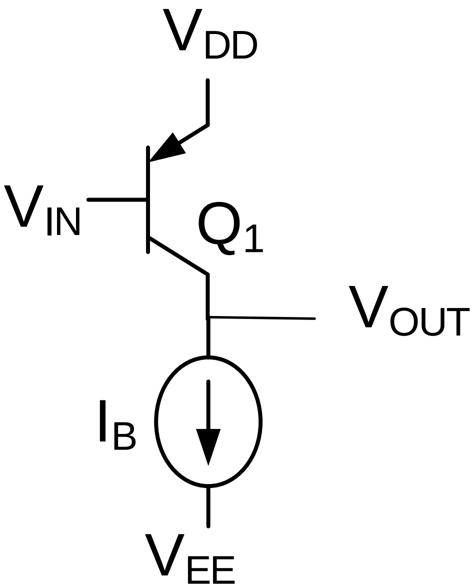
And no design parameters affect the gain

But how can we make a current source?

High-gain amplifier



$$A_V \cong -8000$$

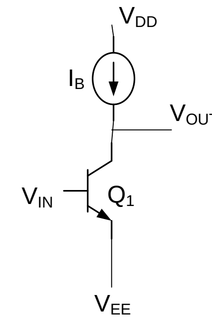


Same gain with both npn and pnp transistors

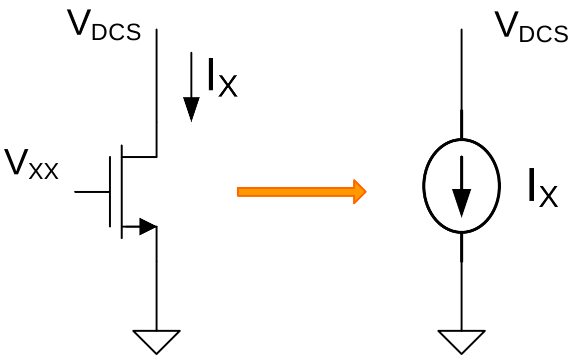
How can we build the ideal current source?

What is the small-signal model of an actual current source?

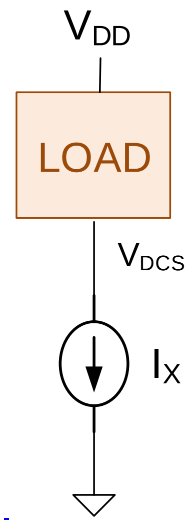
Simple Current Sources



a "sinking" current source



$$I_X = \frac{\mu C_{OX} W}{2L}(V_{XX} - V_T)^2$$



Since I_X is independent of V_{DCS}, acts as an ideal current source (with this model)

Termed a "sinking" current source since current is pulled out of the load

If V_{XX} is available, each dc current source requires only one additional transistor !

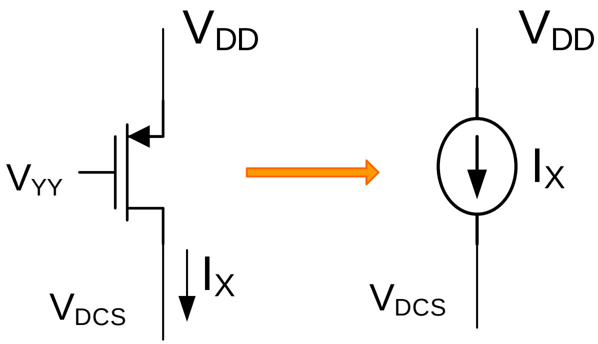
Have several methods for generating V_{XX} from V_{DD} (see HW problems)

But for the npn high-gain amplifier considered need a sourcing current

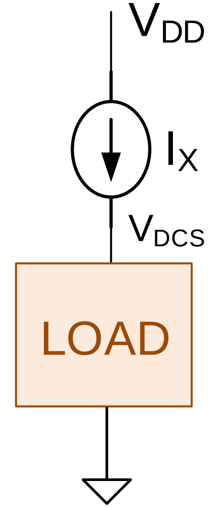
But how good is this current "sink"?

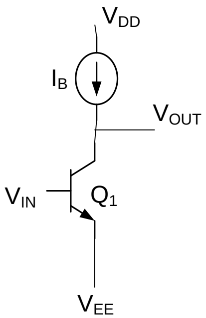
Simple Current Sources

a “sourcing” current source



$$I_X = \frac{\mu C_{OX} W}{2L}\left(V_{DD} - V_{YY} + V_{Tp}\right)^2$$





Since I_X is independent of V_{DCS}, acts as an ideal current source (with this model)

Termed a “sourcing” current source since pushed into the load

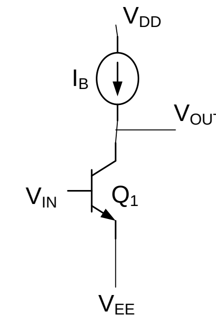
If V_{YY} is available, each dc current source requires only one additional transistor !

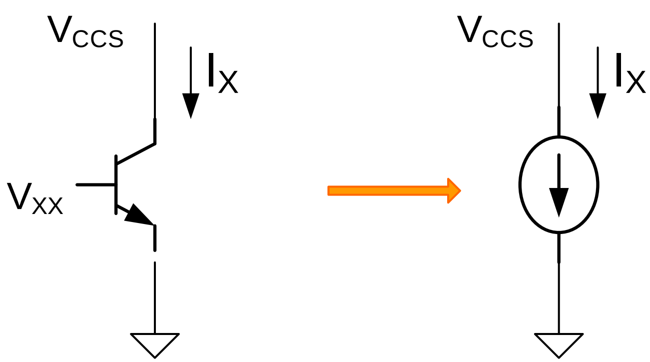
Have several methods for generating V_{YY} from V_{DD} (see HW problems)

But how good is this current “source”?

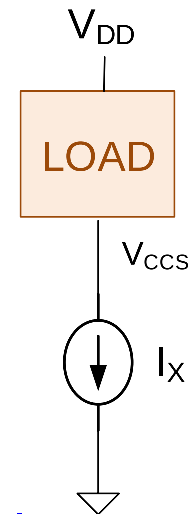
Simple Current Sources

a "sinking" current source





$$I_X = J_S A_E e^{\frac{V_{XX}}{V_t}}$$



Since I_X is independent of V_{CCS}, acts as an ideal current source (with this model)

Termed a "sinking" current source since current is pulled out of the load

If V_{XX} is available, each dc current source requires only one additional transistor !

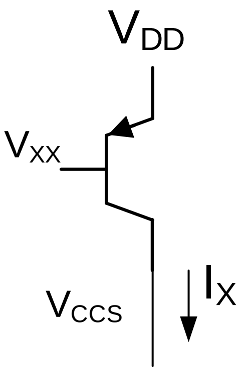
Have several methods for generating V_{XX} from V_{DD} (see HW problems)

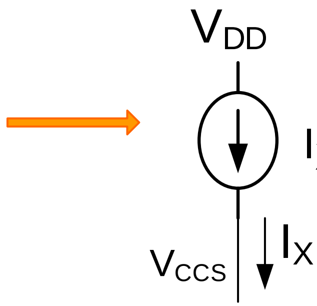
But for the npn high-gain amplifier considered need a sourcing current

But how good is this current "sink"?

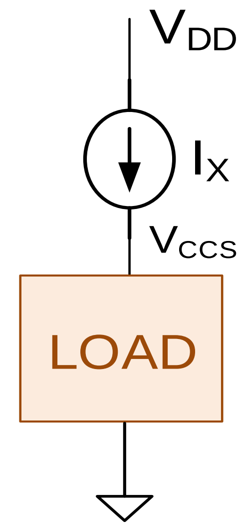
Simple Current Sources

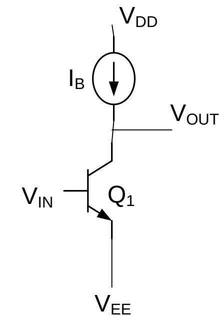
a "sourcing" current source





$$I_X = J_S A_E e^{\frac{V_{DD}-V_{XX}}{V_t}}$$





Since I_X is independent of V_{CCS}, acts as an ideal current source (with this model)

Termed a "sourcing" current source since pushed into the load

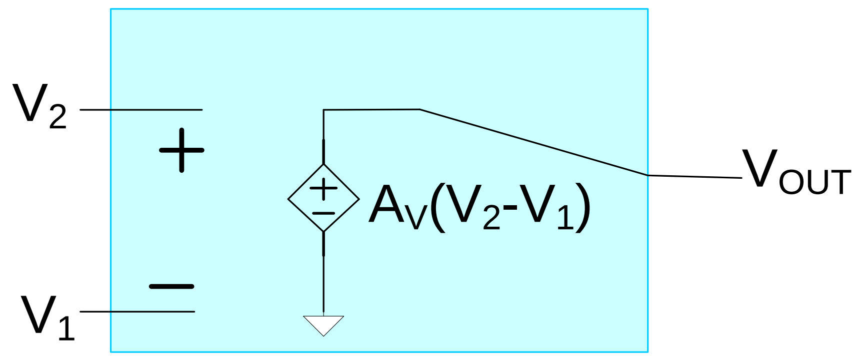
If V_{XX} is available, each dc current source requires only one additional transistor !

Have several methods for generating V_{XX} from V_{DD} (see HW problems)

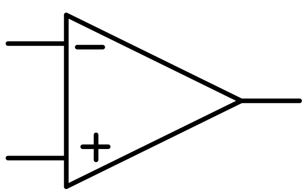
But how good is this current "source"?

Before addressing the issue of how a current source is designed, will consider another circuit that uses current source biasing

The Basic Differential Amplifier

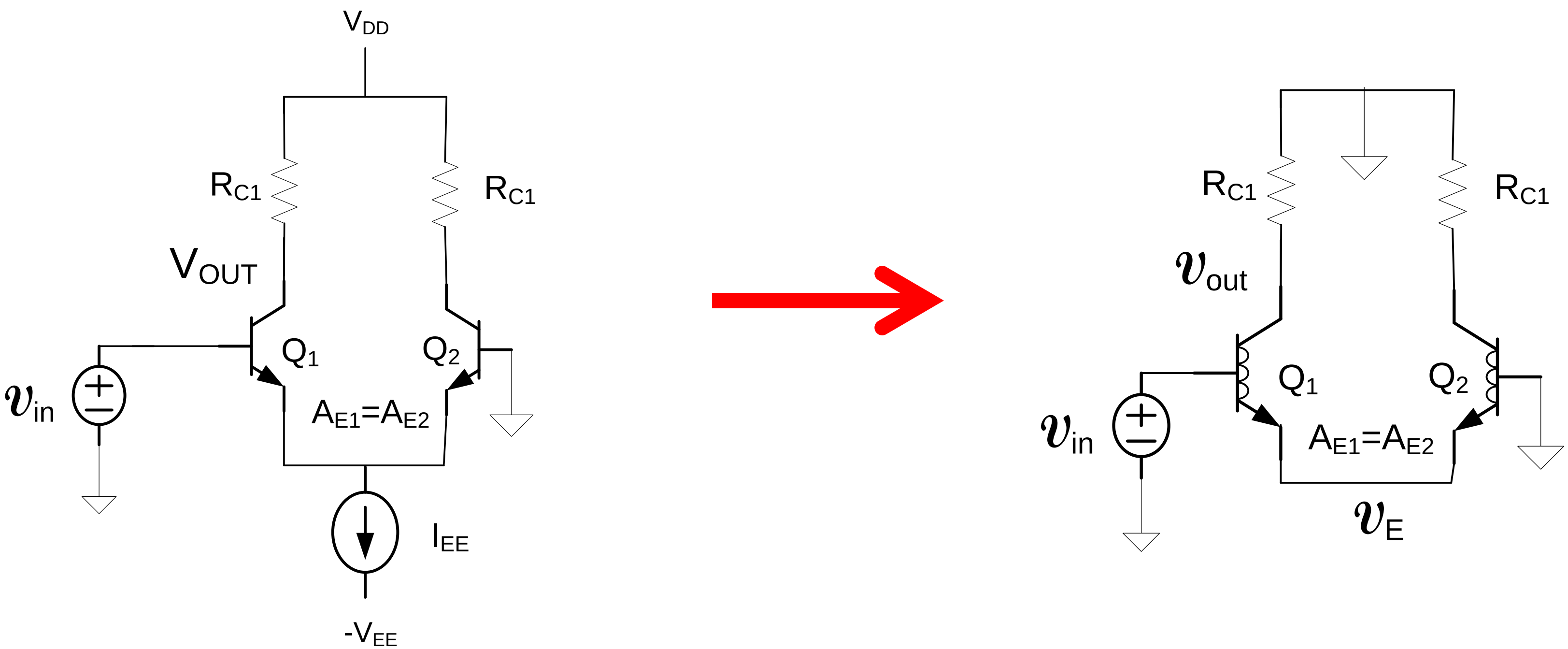


If A_V is large



Operational Amplifier (Op Amp)

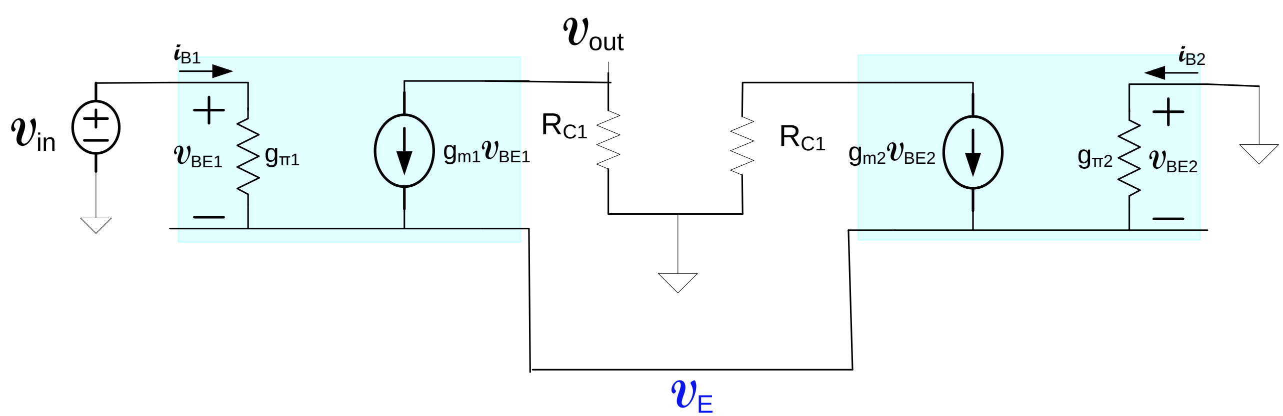
Example: Determine the voltage gain of the following circuit



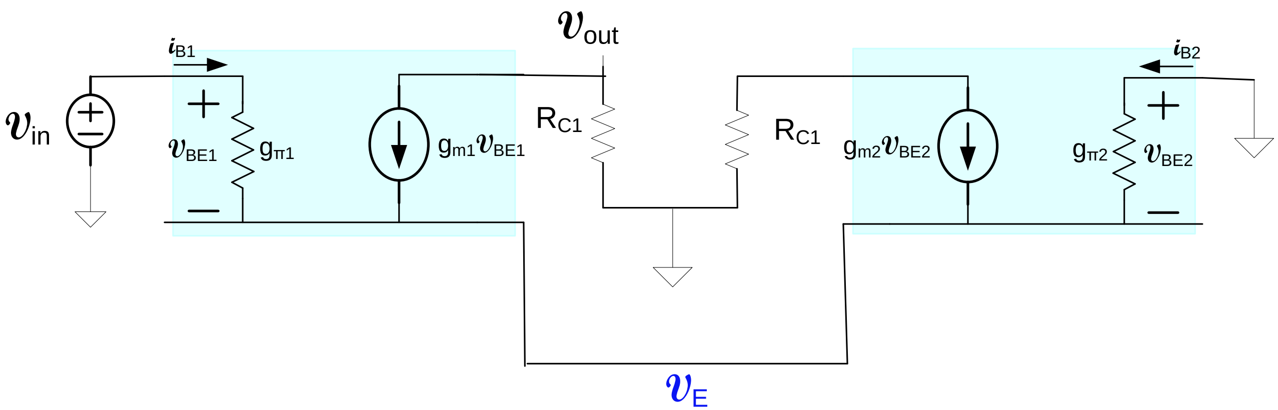
Since symmetric when v_{IN}=0

$$I_{C1} = I_{C2} = \frac{I_{EE}}{2}$$

$$g_{m1} = g_{m2} = \frac{I_{EE}}{2V_t}$$



Example: Determine the voltage gain of the following circuit



$$v_E\left(g_{\pi1}+g_{\pi1}\right)=g_{\pi1}v_{IN}+g_{m1}\left(v_{IN}-v_E\right)+g_{m2}\left(-v_E\right)$$

$$v_{OUT}=-R_{C1}g_{m1}\left(v_{IN}-v_E\right)$$

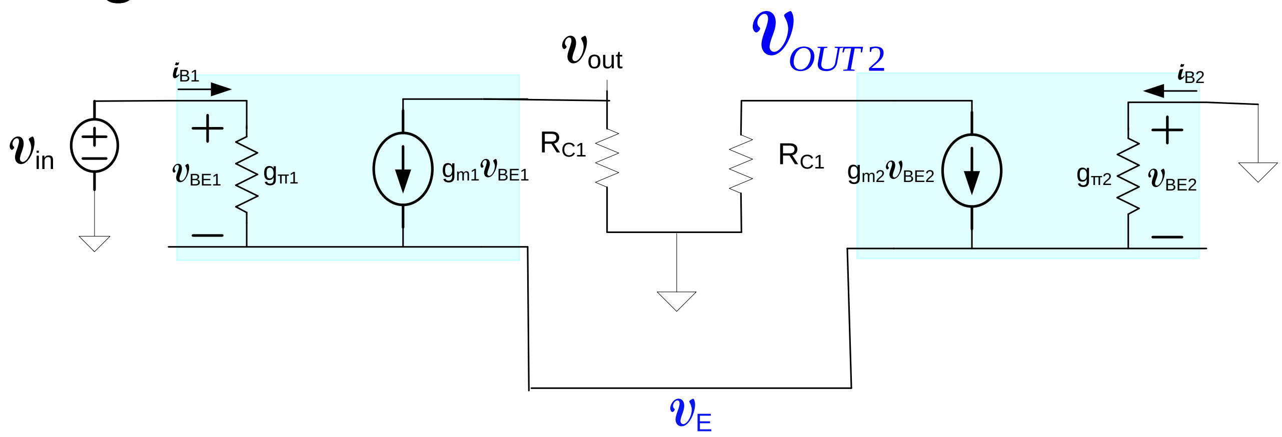
$$v_E\left(g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}\right)=v_{IN}\left(g_{m1}+g_{\pi1}\right)$$

$$v_E=\frac{\left(g_{m1}+g_{\pi1}\right)}{\left(g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}\right)}v_{IN}$$

$$v_{OUT}=-R_{C1}g_{m1}v_{IN}\left[1-\frac{\left(g_{m1}+g_{\pi1}\right)}{\left(g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}\right)}\right]$$

$$v_{OUT}=-R_{C1}g_{m1}v_{IN}\left[\frac{g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}-\left(g_{m1}+g_{\pi1}\right)}{\left(g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}\right)}\right]$$

Example: Determine the voltage gain of the following circuit



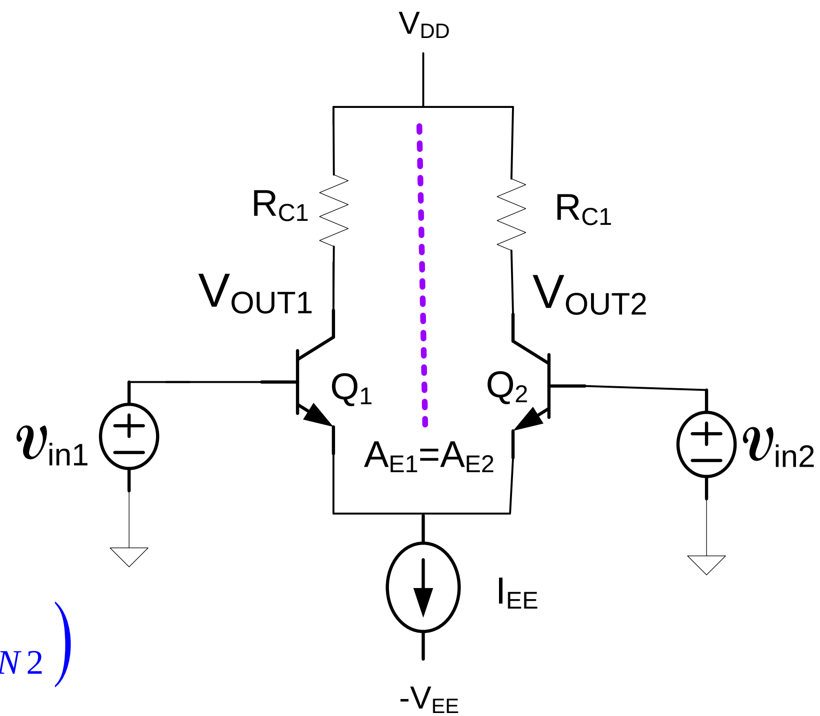
$$v_{OUT} = -R_{C1}g_{m1}v_{IN}\left[\frac{g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}-\left(g_{m1}+g_{\pi1}\right)}{\left(g_{\pi1}+g_{\pi2}+g_{m1}+g_{m2}\right)}\right]$$

$$v_{OUT} \cong -R_{C1}g_{m1}v_{IN}\left[\frac{g_{m2}}{\left(g_{m1}+g_{m2}\right)}\right]$$

$$v_{OUT} \cong \left[\frac{-R_{C1}g_{m1}}{2}\right]v_{IN}$$

$$v_{OUT2} \cong \left[\frac{R_{C1}g_{m1}}{2}\right]v_{IN}$$

Differential amplifier

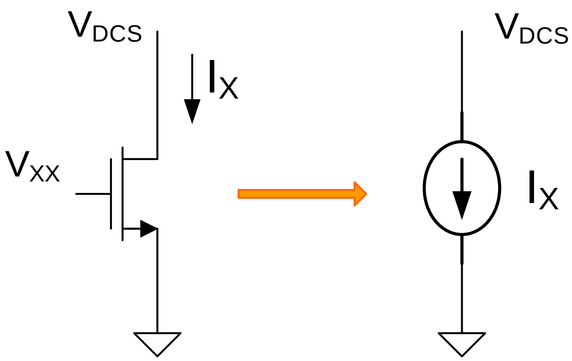


$$v_{OUT1} \cong -\left[\frac{R_{C1}g_{m1}}{2}\right]\left(v_{IN1} - v_{IN2}\right)$$

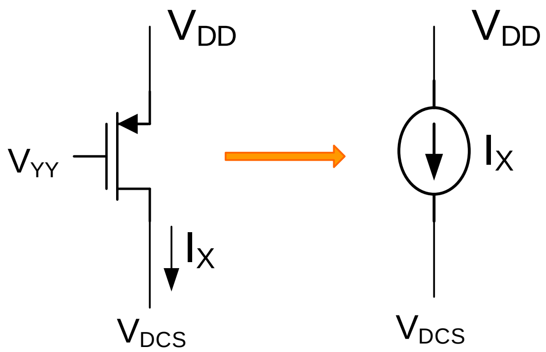
$$v_{OUT2} \cong \left[\frac{R_{C1}g_{m1}}{2}\right]\left(v_{IN1} - v_{IN2}\right)$$

- Very useful circuit
- This is a basic Op Amp
- Uses a current source and V_{DD} for biasing (no biasing resistors or caps!)
- But – needs a dc current source !!!!

Simple Current Sources



$$I_X = \frac{\mu C_{OX} W}{2L}\left(V_{XX} - V_T\right)^2$$



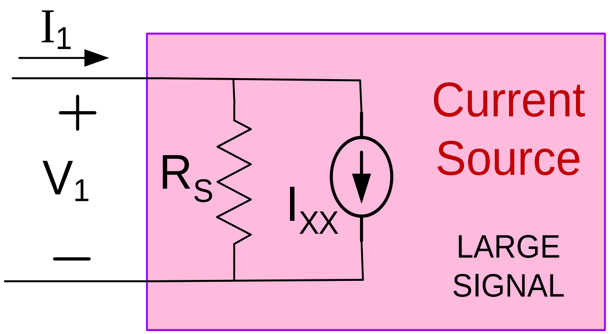
$$I_X = \frac{\mu C_{OX} W}{2L}\left(V_{DD} - V_{YY} + V_{Tp}\right)^2$$

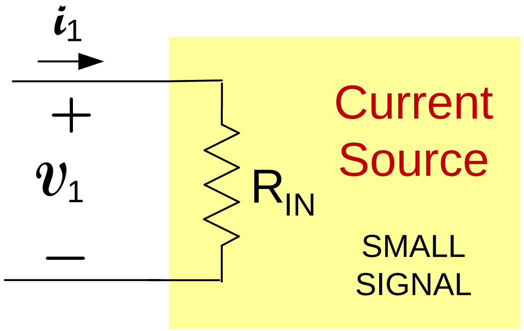
But how good are these current sources?

Model of dc Current Source

"Reasonable dc Current Source"

Small-signal model of dc current source (since one-port)

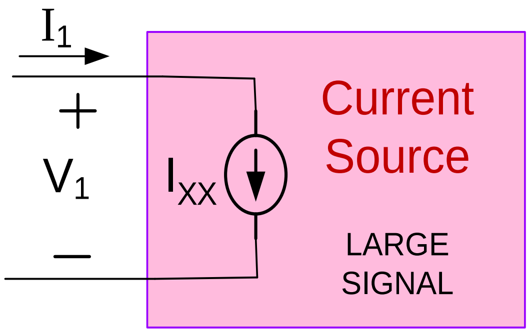


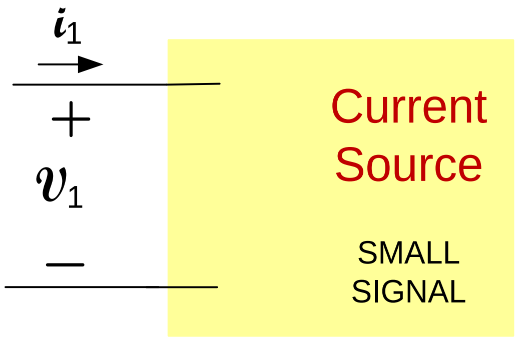


I_{XX} independent of V_1 and t , R_S large

want R_{IN} large

Ideal dc Current Source



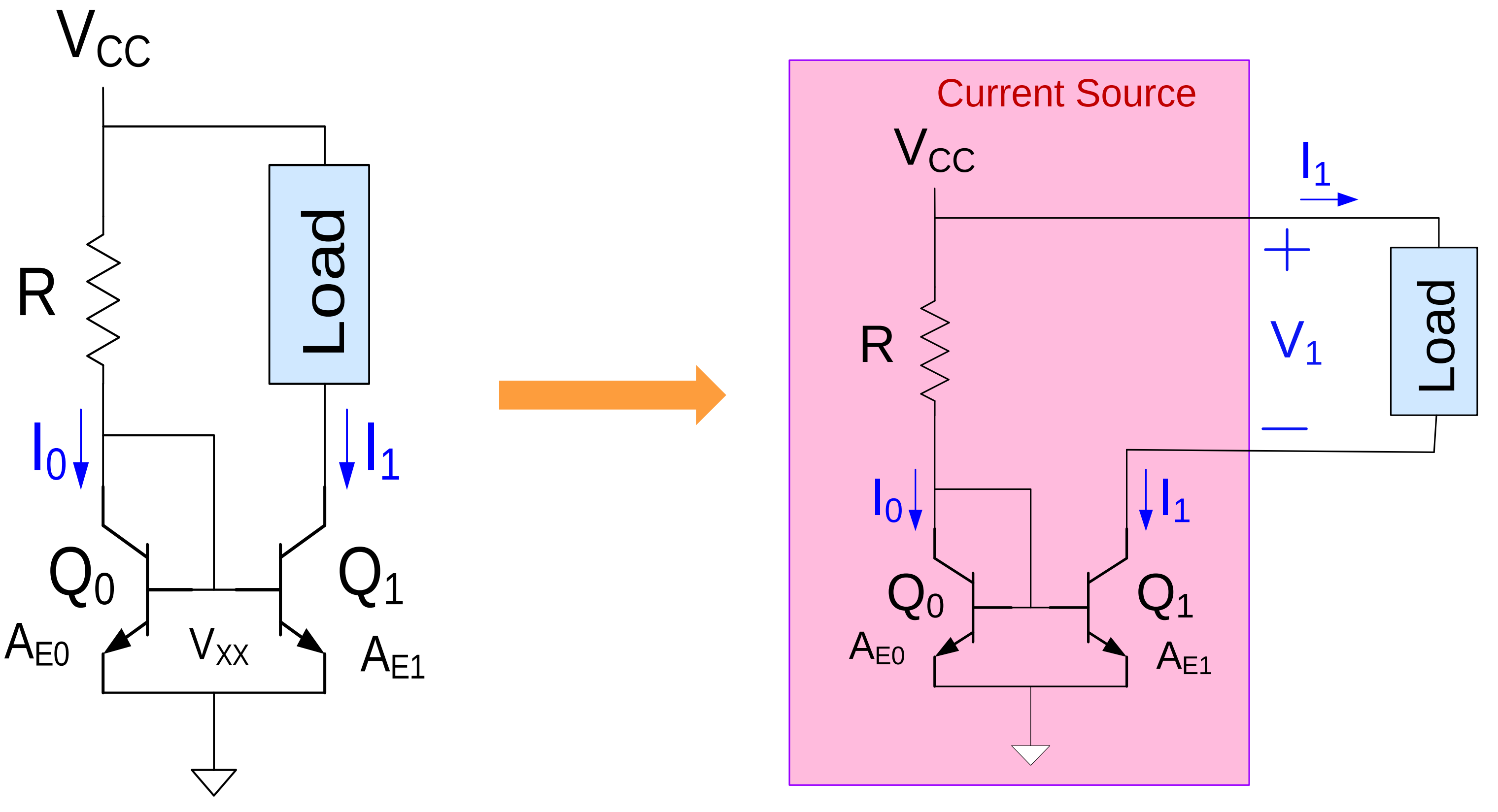


I_{XX} independent of V_1 and t

$R_{IN}=\infty$

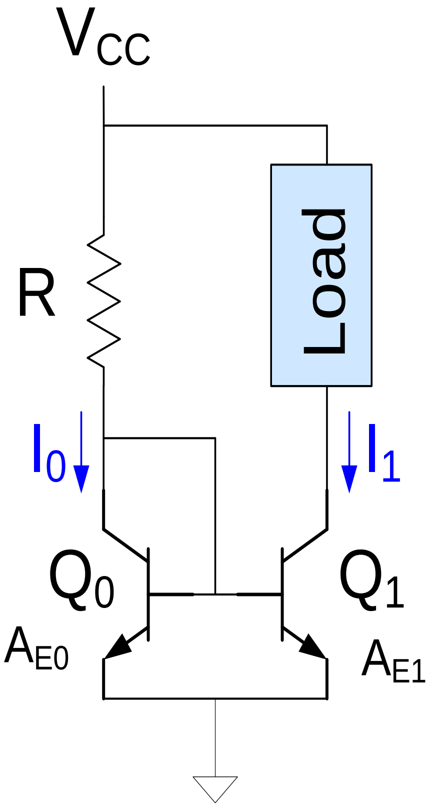
Current Sources/Mirrors

Will show circuit in red behaves as a current source



R and Q_0 simply generate voltage V_{XX} in previous circuit

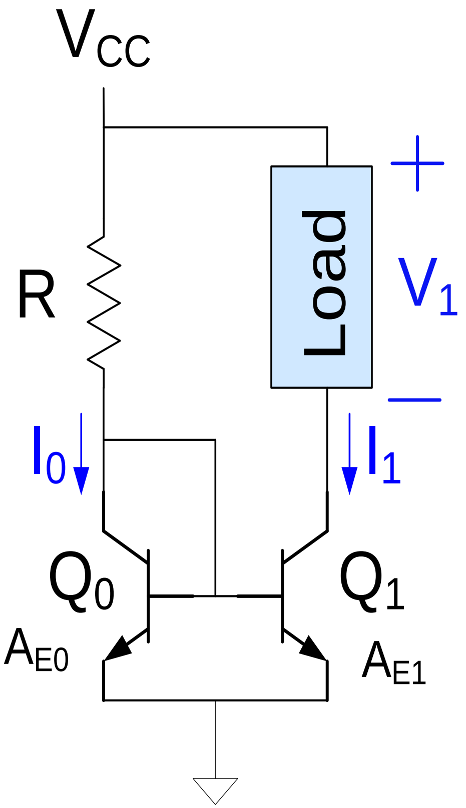
Current Sources/Mirrors



$$I_0 \cong \frac{(V_{CC} - 0.6V)}{R}$$

If the base currents are neglected

Current Sources/Mirrors



$$I_0 \cong \frac{(V_{CC} - 0.6V)}{R}$$

If the base currents are neglected

$$I_0 = J_S A_{E0} e^{\frac{V_{BE0}}{V_t}}$$

$$I_1 = J_S A_{E1} e^{\frac{V_{BE1}}{V_t}}$$

since $V_{BE1}=V_{BE2}$

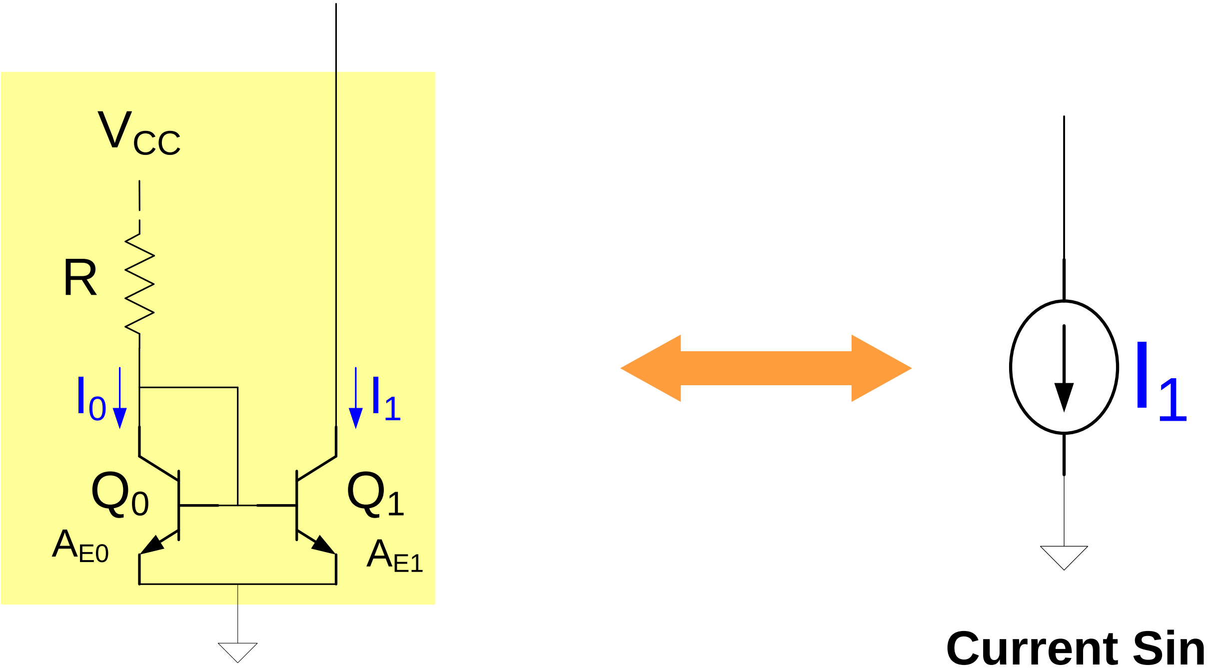
$$I_1 \cong \left(\frac{A_{E1}}{A_{E0}}\right) I_0 = \left(\frac{A_{E1}}{A_{E0}}\right) \frac{V_{CC} - 0.6V}{R}$$

Note I_1 is not a function of V_1

Behaves as a current sink ! So is ideal with this model !!

And does not require an <u>additional</u> dc voltage source !!!

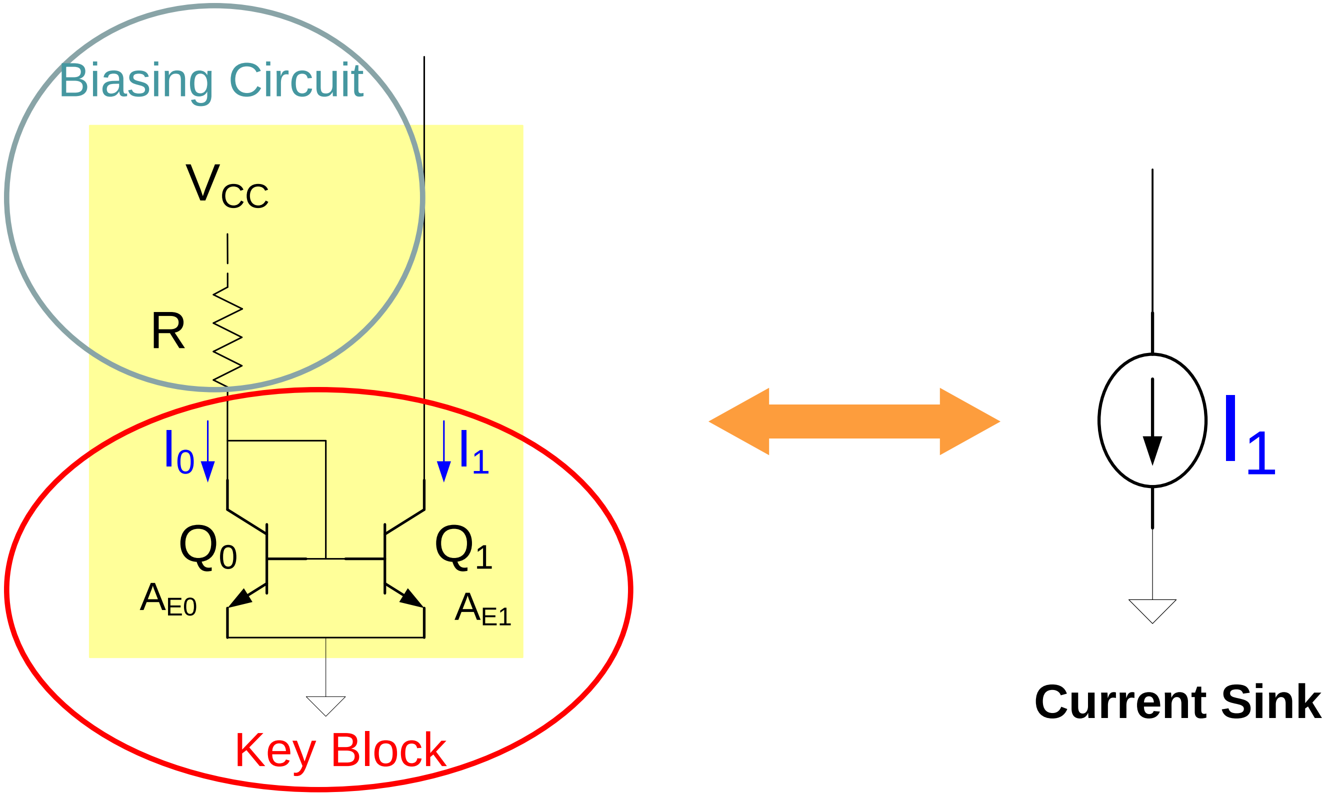
Current Sources/Mirrors



Current Sink

- **Multiple Outputs Possible**
- **Can be built for sourcing or sinking currents**
- **Also useful as a current amplifier**
- **MOS counterparts work very well and are not plagued by base current**

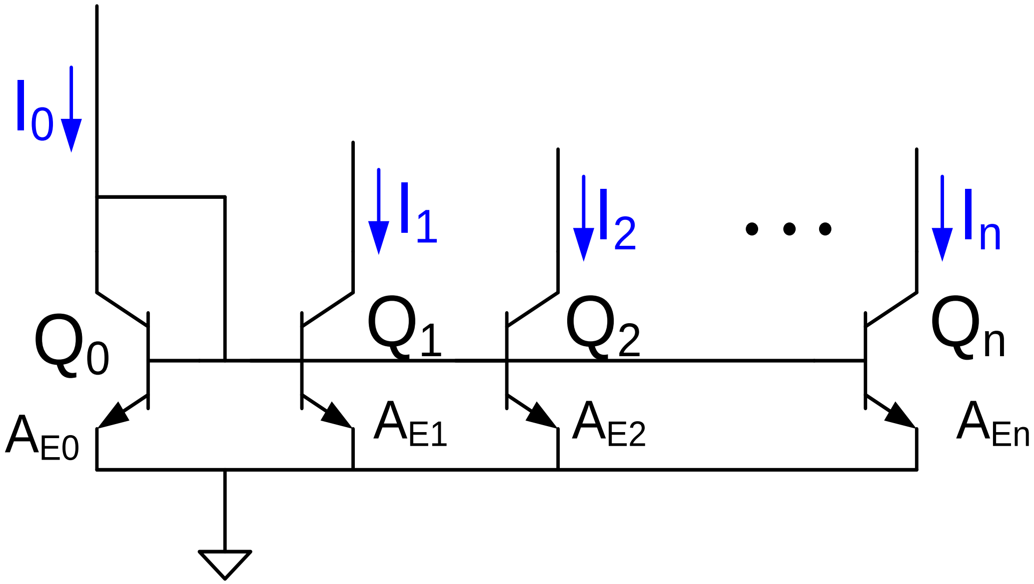
Current Sources/Mirrors



Two ways to look at this circuit:

- Q_0 and R bias Q_1
- R biases the $Q_0 : Q_1$ block

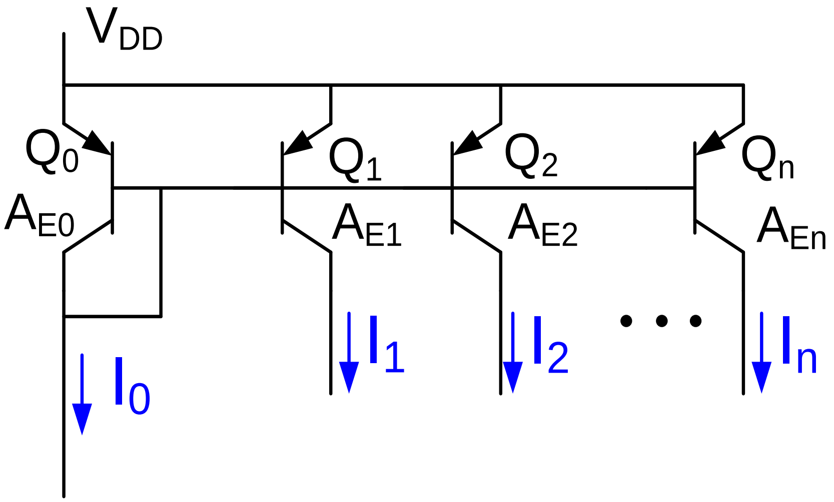
Current Sources/Mirrors



Multiple-Output Bipolar Current Sink

$$I_k = \left[\frac{A_{Ek}}{A_{E0}} \right] I_0$$

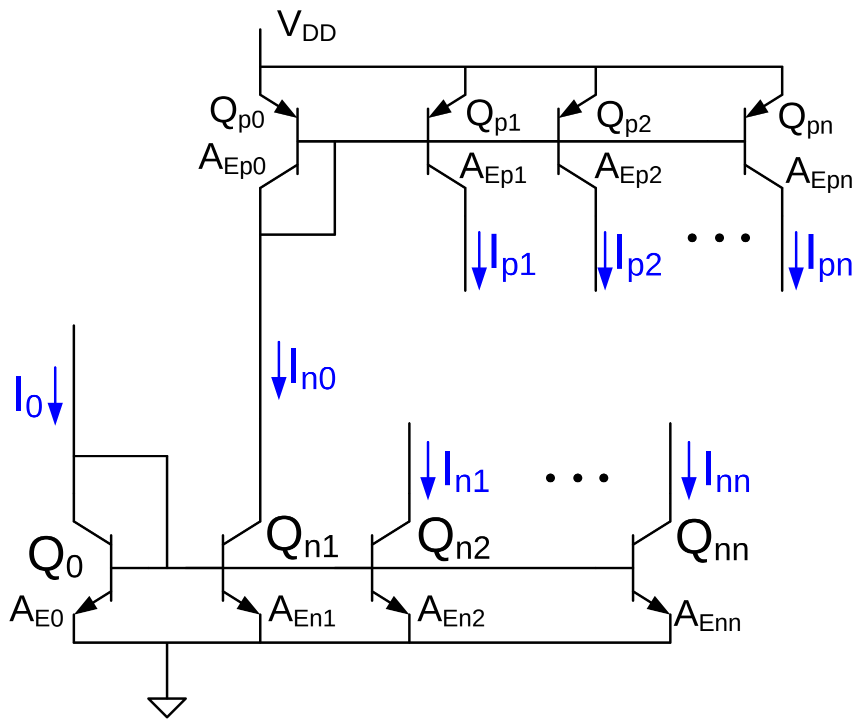
Current Sources/Mirrors



Multiple-Output Bipolar Current Source

$$I_k = \left[\frac{A_{Ek}}{A_{E0}}\right] I_0$$

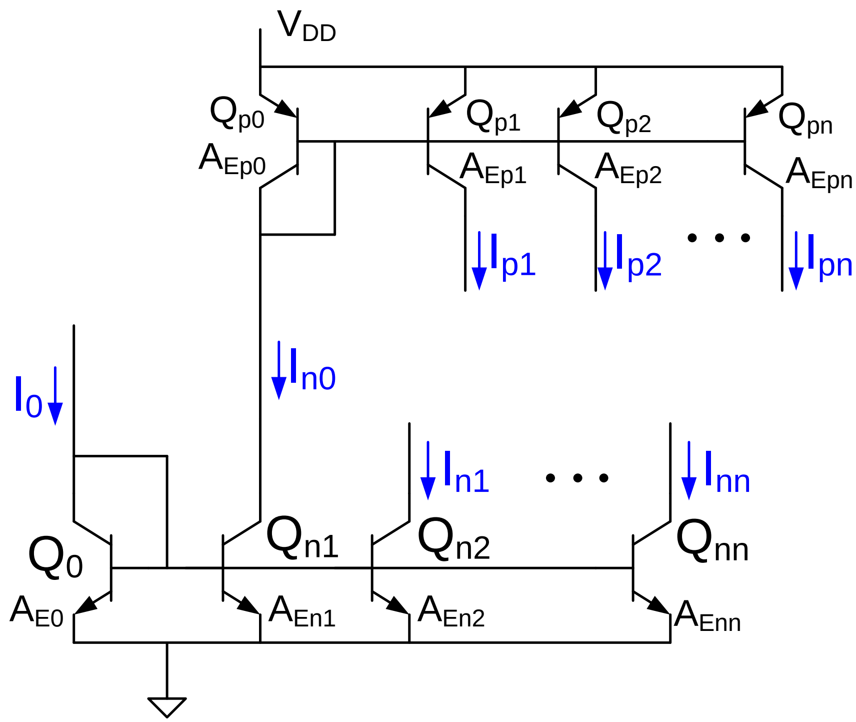
Current Sources/Mirrors



Multiple-Output Bipolar Current Source and Sink

I_{nk} =? I_{pk} =?

Current Sources/Mirrors

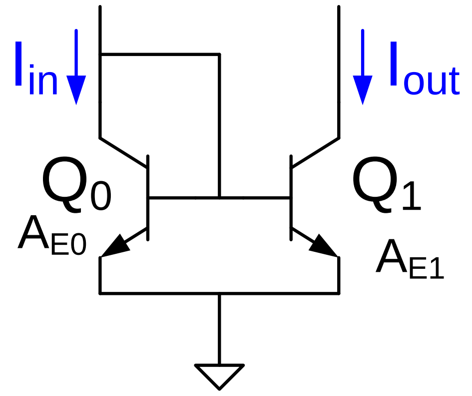


Multiple-Output Bipolar Current Source and Sink

$$I_{nk} = \left[\frac{A_{Enk}}{A_{E0}}\right] I_0$$

$$I_{pk} = \left[\frac{A_{En1}}{A_{E0}}\right]\left[\frac{A_{Epk}}{A_{Ep0}}\right] I_0$$

Current Sources/Mirrors



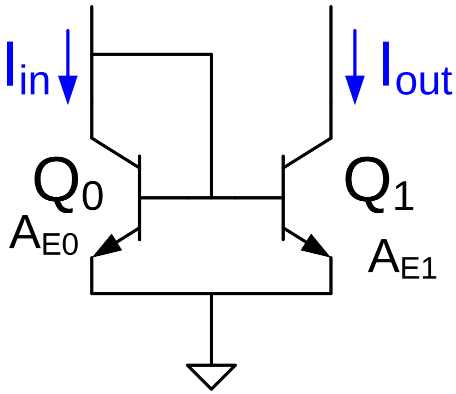
npn Current Mirror

$$I_{out} = \left[\frac{A_{E1}}{A_{E0}} \right] I_{in}$$

- **Termed a "current mirror"**
- **Output current linearly dependent on I_{in}**
- **Serves as a current amplifier**
- **Widely used circuit**

But I_{in} and I_{out} must be positive !

Current Sources/Mirrors



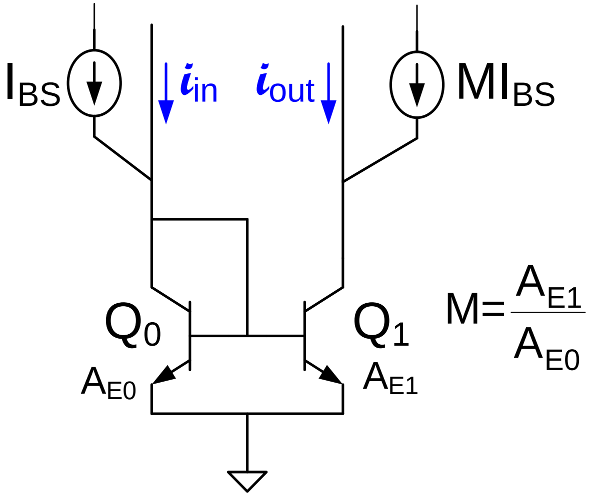
npn Current Mirror

$$I_{out} = \left[\frac{A_{E1}}{A_{E0}}\right] I_{in}$$

- **Termed a "current mirror"**
- **Output current linearly dependent on I_{in}**
- **Small-signal and large-signal relationships the same since linear**
- **Serves as a current amplifier**
- **Widely used circuit**

But I_{in} must be positive !

Current Sources/Mirrors



npn current mirror amplifier

i_{out}=?

$$\frac{i_{OUT}+MI_{BS}}{i_{in}+I_{BS}}=M$$

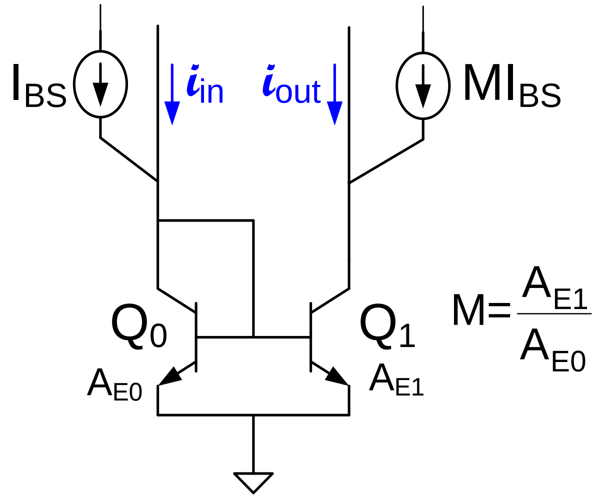
$$i_{OUT}+MI_{BS}=M\left(i_{in}+I_{BS}\right)$$

$$i_{OUT}+M\cancel{I}_{BS}=M\left(i_{in}+\cancel{I}_{BS}\right)$$

$$\frac{i_{OUT}}{i_{in}}=M$$

But $I_{BS}+i_{in}>0$!

Current Sources/Mirrors



npn current mirror amplifier

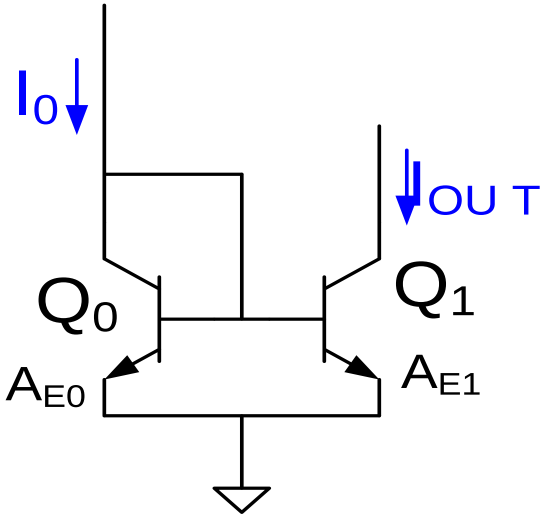
$$\boldsymbol{i}_{out} = \left[\frac{A_{E1}}{A_{E0}}\right]\boldsymbol{i}_{in}$$

Amplifiers both positive and negative currents (provided $i_{IN}>-I_{BS}$)

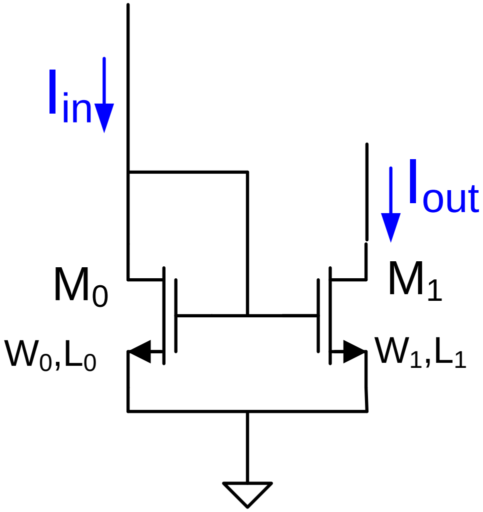
Current amplifiers are easy to build !!

Current gain can be accurately controlled with appropriate layout !!

Current Sources/Mirrors



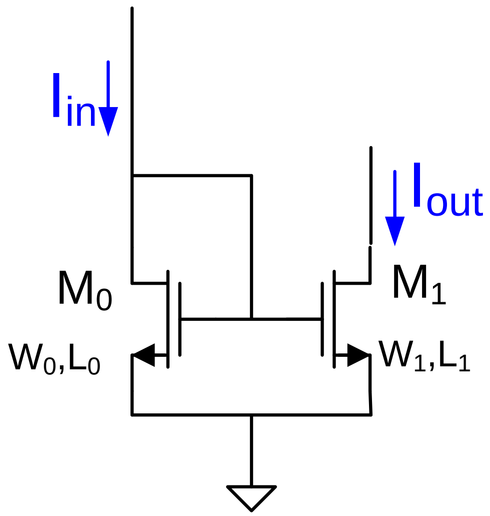
npn Current Mirror



n-channel Current Mirror

$I_{out} = ?$

Current Sources/Mirrors



n-channel Current Mirror

$$I_{in}=\frac{\mu C_{OX}W_0}{2L_0}\left(V_{GS0}-V_{T0}\right)^2$$

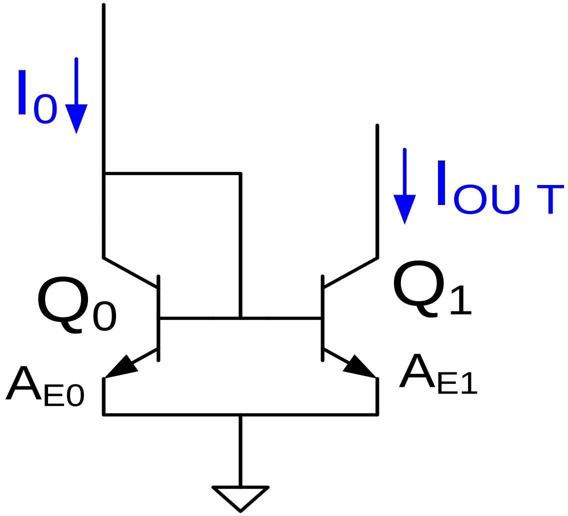
$$I_{out}=\frac{\mu\, C_{OX}W_1}{2L_1}\left(V_{GS1}-V_{T1}\right)^2$$

If process parameters are matched, it follows that

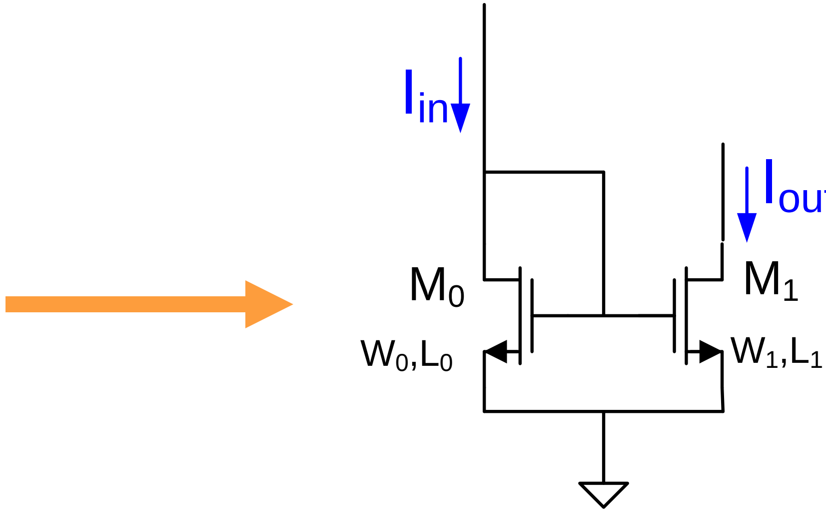
$$I_{out}=\left[\frac{W_1}{W_0}\frac{L_0}{L_1}\right]I_{in}$$

- Current mirror gain <u>can</u> be accurately controlled !
- Layout is important to get accurate gain (for both MOS and BJT)

Current Sources/Mirrors Summary



npn Current Mirror

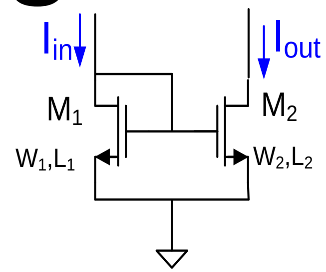


n-channel Current Mirror

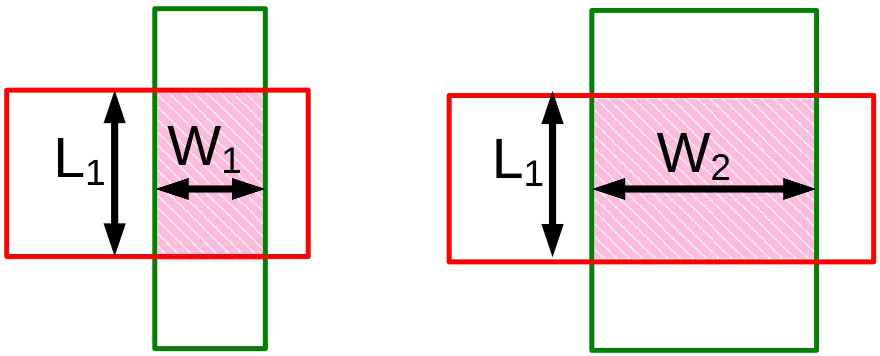
$$I_{out} = \left[\frac{A_{E1}}{A_{E0}} \right] I_{in}$$

$$I_{out} = \left[\frac{W_1}{W_0} \frac{L_0}{L_1} \right] I_{in}$$

Layout of Current Mirrors

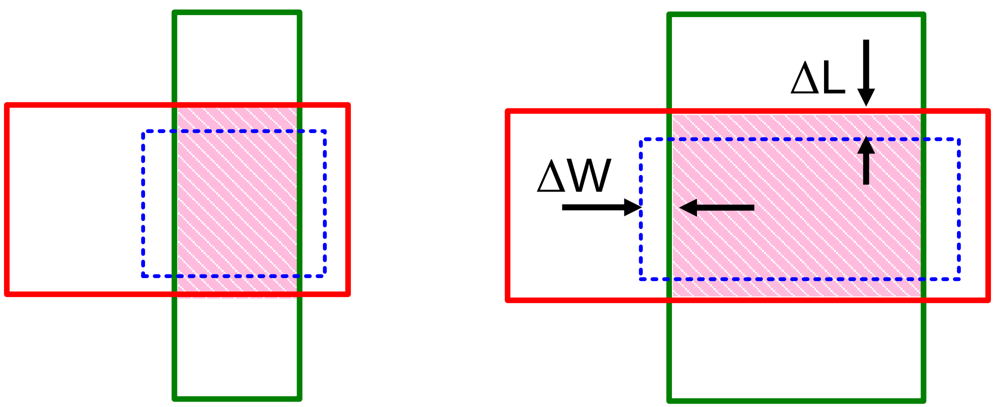


Example with M = 2



$$M = \left[\frac{W_2}{W_1} \frac{L_1}{L_2} \right]$$

Standard layout



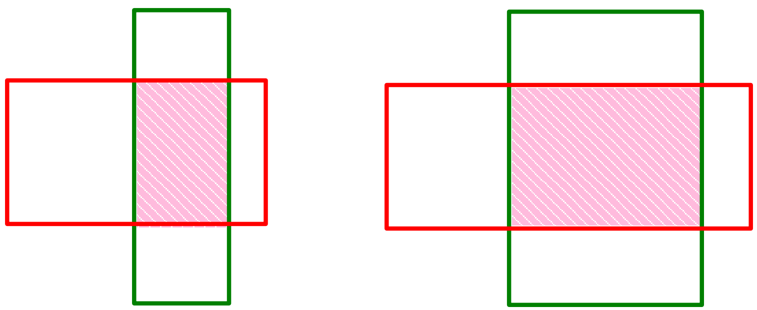
$$M = \left[\frac{W_2 + 2\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_2 + 2\Delta L} \right]$$

$$M = \left[\frac{2W_1 + 2\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L} \right] \neq 2$$

Gate area after fabrication depicted

Layout of Current Mirrors

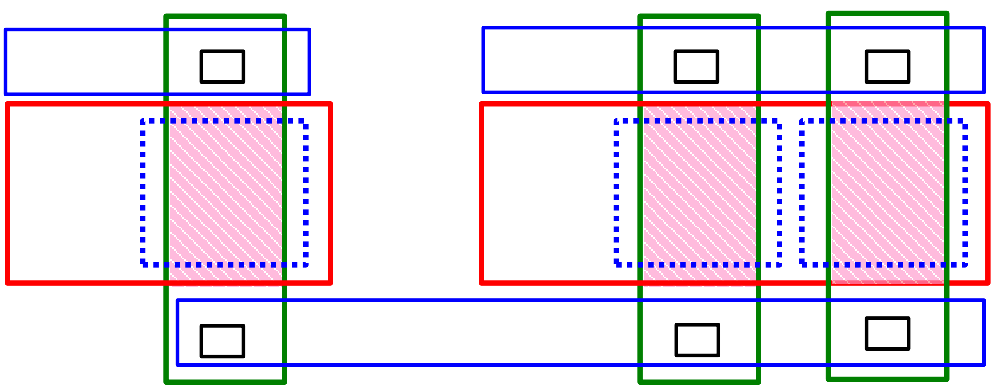
Example with M = 2



Standard layout

$$M=\left[\frac{W_2}{W_1}\frac{L_1}{L_2}\right]$$

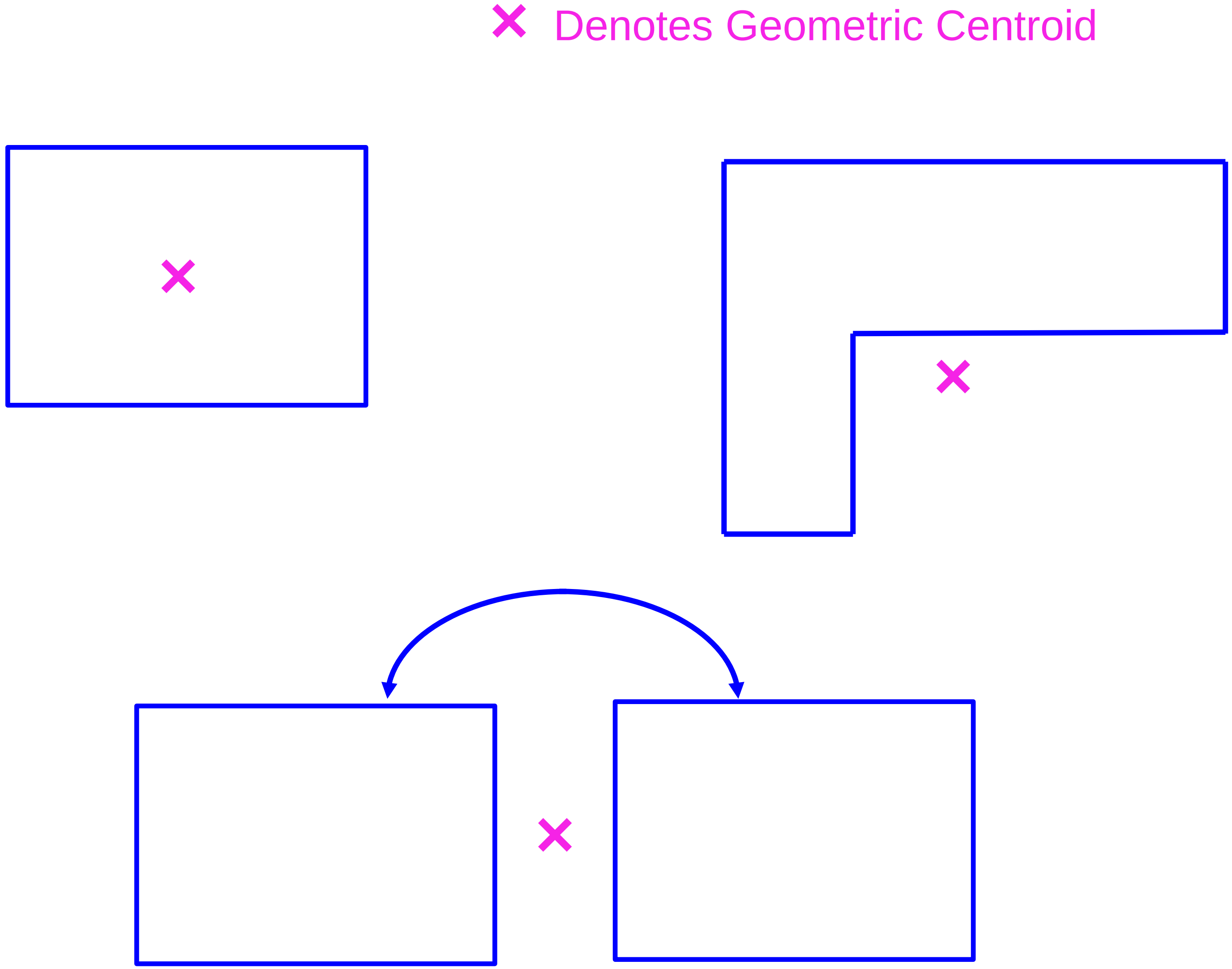
$$M=\left[\frac{2W_1+2\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]\neq 2$$



Better Layout

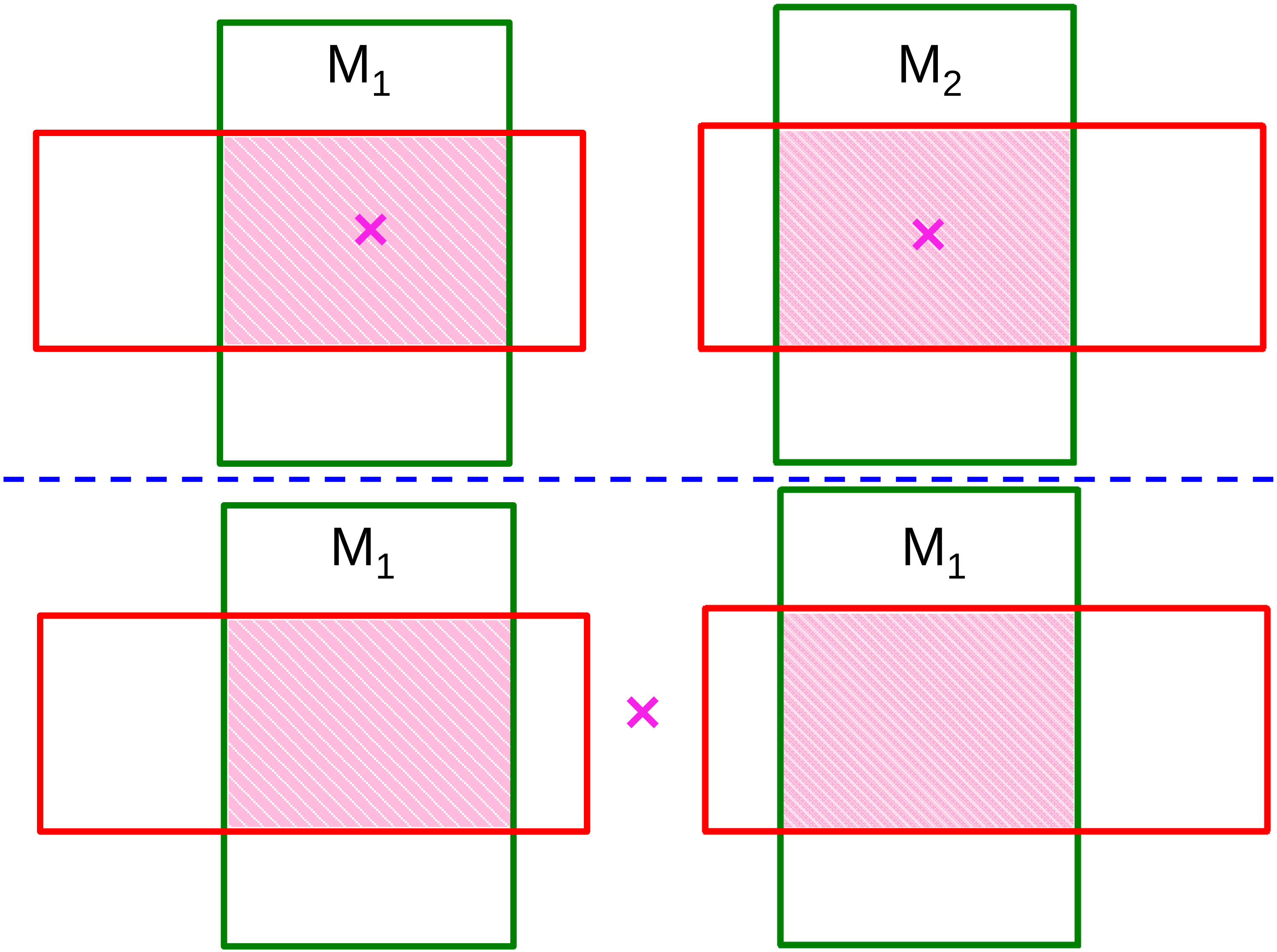
$$M=\left[\frac{2W_1+4\Delta W}{W_1+2\Delta W}\bullet\frac{L_1+2\Delta L}{L_1+2\Delta L}\right]=2$$

Centroid and Common Centroid

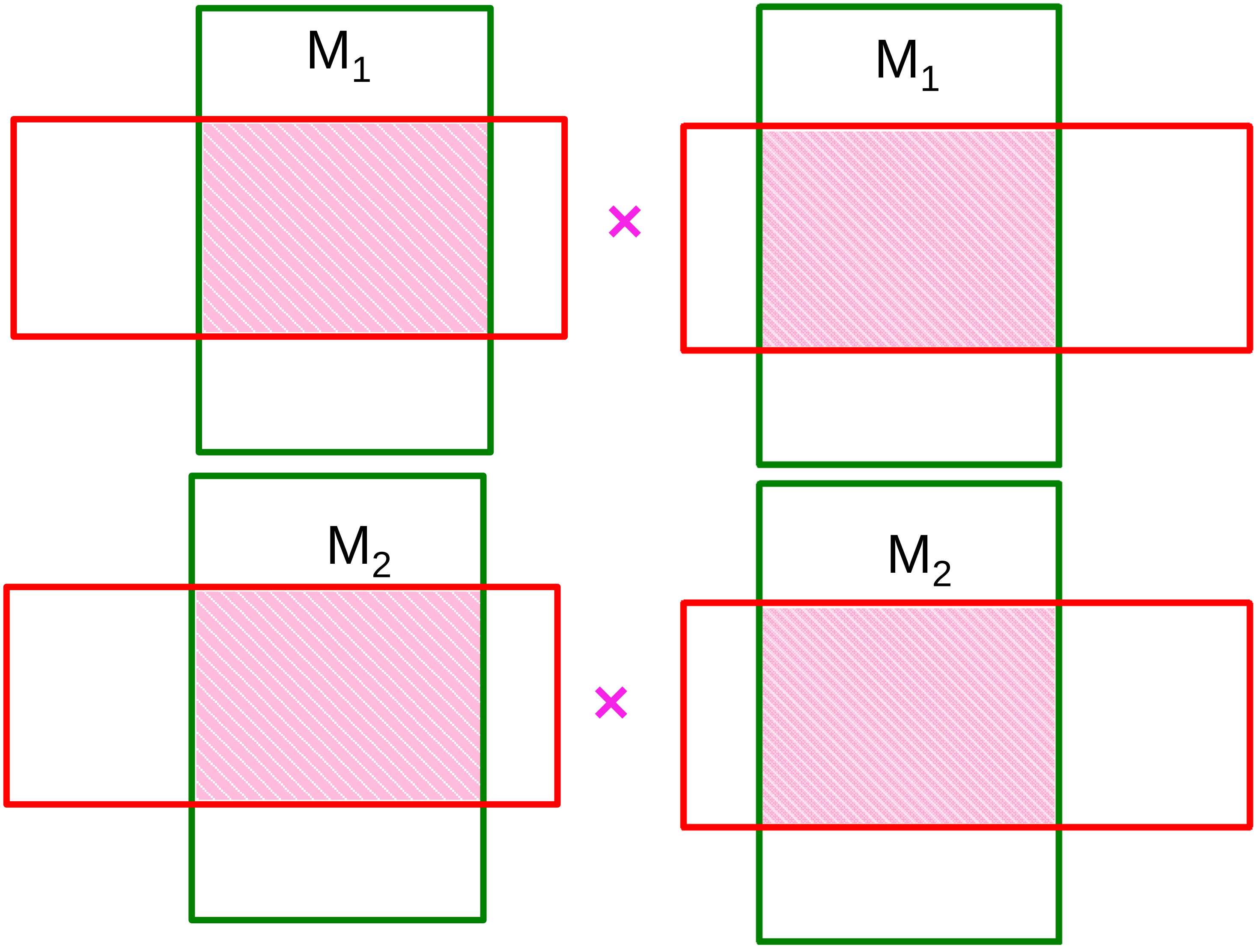


Centroid and Common Centroid

Geometric Centroids of Channel

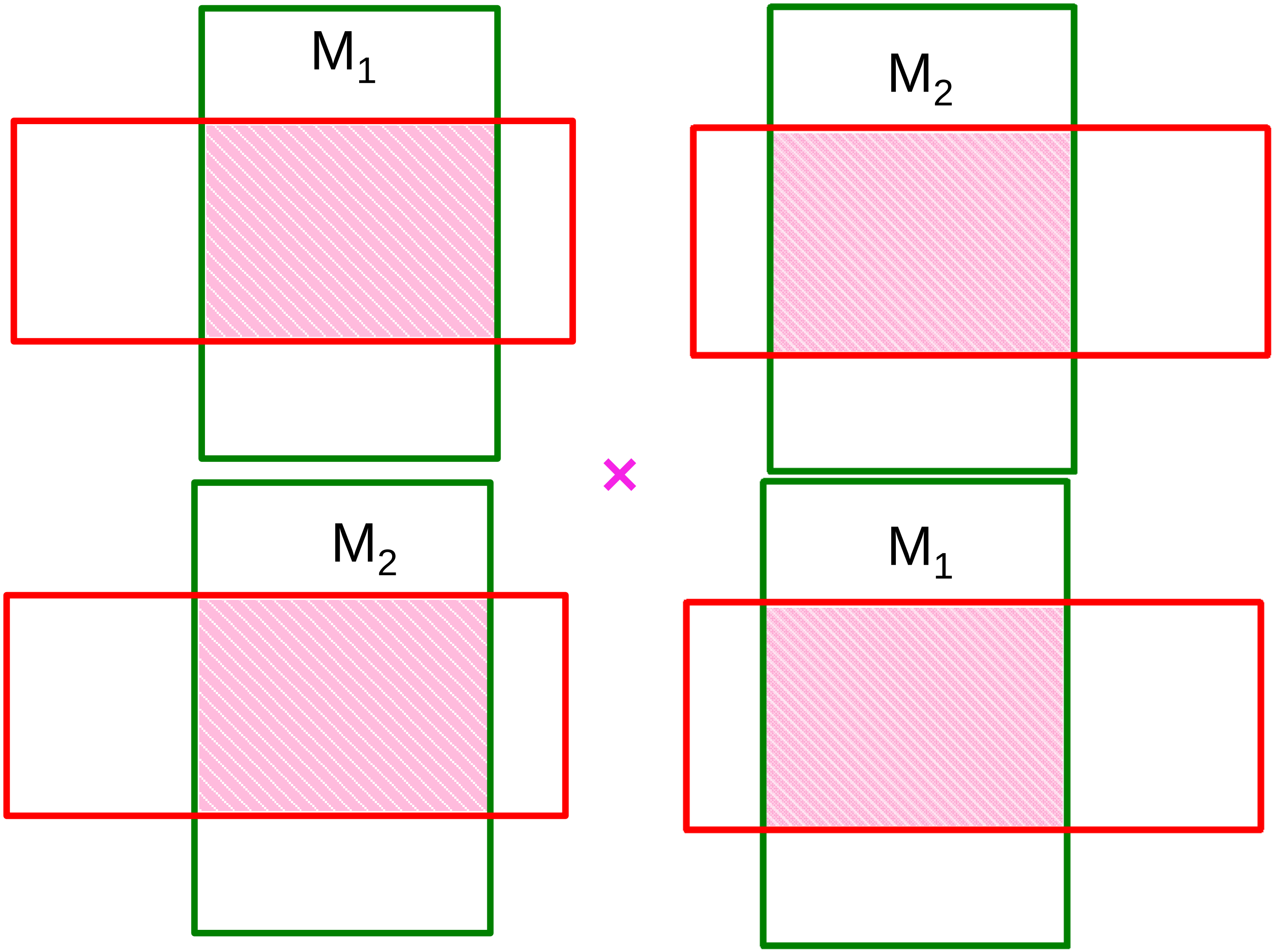


Centroid and Common Centroid



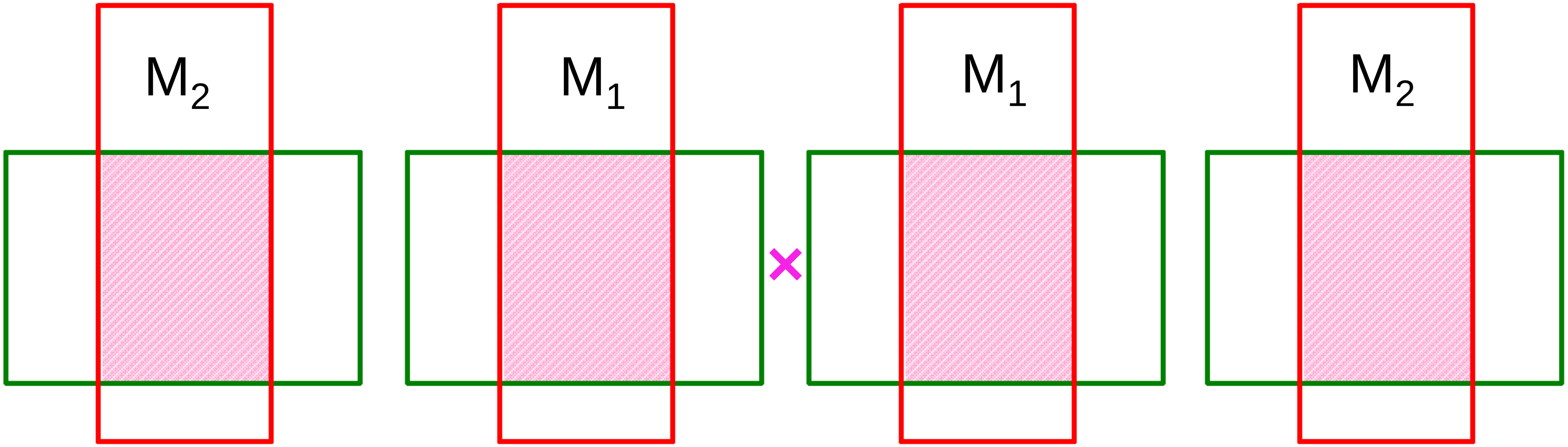
Centroid and Common Centroid

Common Centroid for Matched Devices



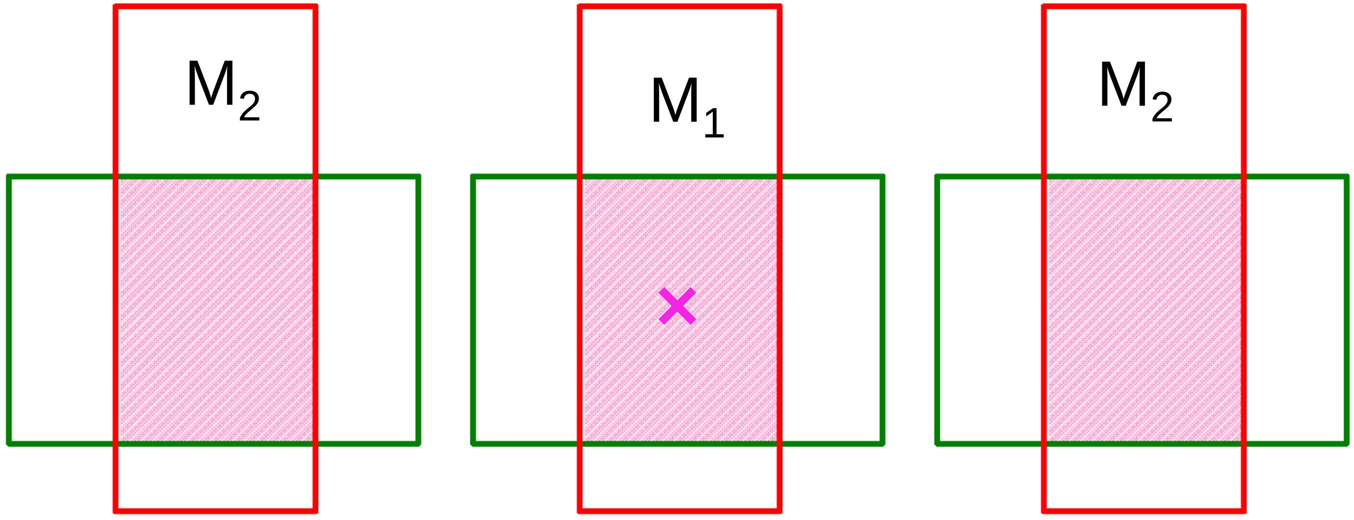
Centroid and Common Centroid

Common Centroid for Matched Devices

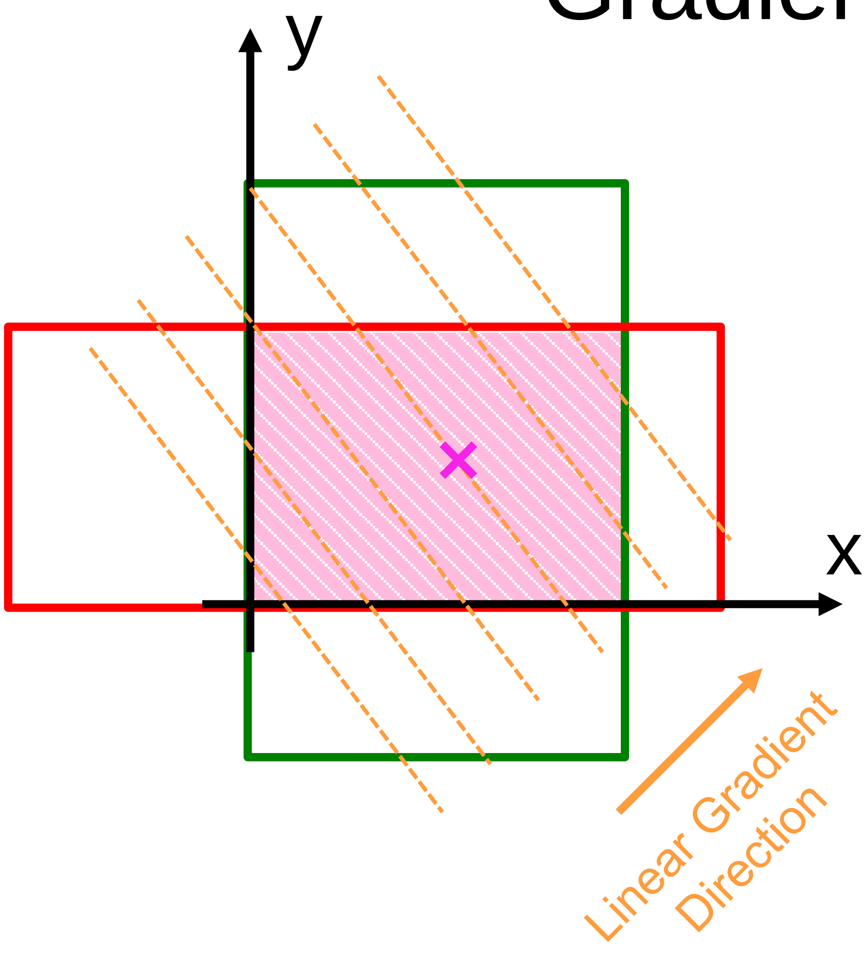


Centroid and Common Centroid

Common Centroid for Ratioed Devices $M = \frac{W_2}{W_1}\frac{L_1}{L_2} = 2$



Gradient



Threshold voltage dependent upon position

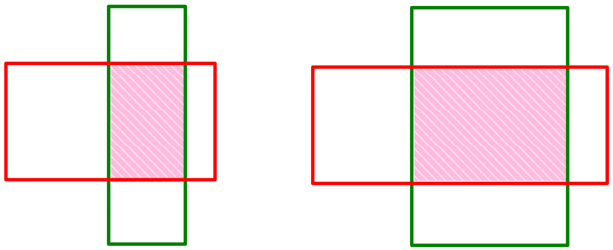
$V_{TH}(x,y)$

For linear gradient, $V_{THEQ}=V_{TH}(X_C,Y_C)$

× : (X_C,Y_C)

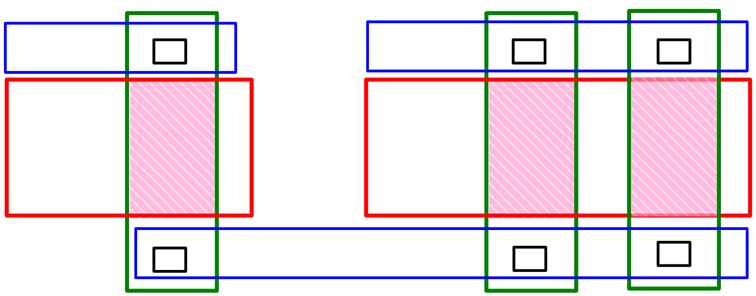
Layout of Current Mirrors

Example with M = 2



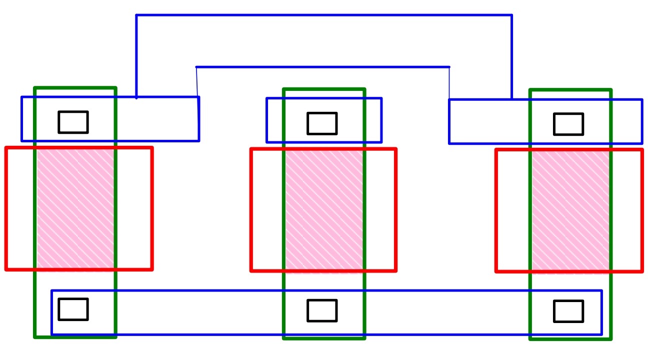
Standard layout

$$M = \left[\frac{W_2}{W_1} \frac{L_1}{L_2} \right]$$



Better Layout

$$M = \left[\frac{2W_1 + 4\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L} \right] = 2$$



Even Better Layout

$$M = \left[\frac{2W_1 + 4\Delta W}{W_1 + 2\Delta W} \bullet \frac{L_1 + 2\Delta L}{L_1 + 2\Delta L} \right] = 2$$

This is termed a common-centroid layout

Stay Safe and Stay Healthy !

End of Lecture 33